DEPARTMETN OF ELECTRICAL & ELECTRONICS ENGINEERING

END OF SEMESTER EXAMINATION -ACADEMIC YEAR 2020-2021

TRIMESTER I

GROUP: Y2 EPE

MODULE: EPE2165—ANALOG ELECTRONICS

DATE: 14/09/2021

TIME: 2 hours

MAX POINTS = 50 POINTS

INSTRUCTIONS

- You have 2 hours to complete the exam. Be a smart test taker: if you get stuck on one problem go on to the next.
- This exam paper comprises 3 pages, excluding the title page. Please check that you have received all of them.
- This exam paper contains 3 questions. Answer only 2 questions as follows
  - QUESTION # 1 is COMPULSORY
  - Chose ONE (1) question from questions 2 and 3
  - If a candidate answers more than two questions, at the sole discretion of the grader, only two questions will be graded.
- Keep your answers short and to the point. Longer is not necessarily better as the number of written words is NOT a grading criterion and, in some case, longer answers may even make your answer abstruse.
- Write legibly. If the grader cannot read it, you will not get credit for it.
- Write all your answers in the answer booklet provided
- Do not forget to write your Registration Number
- No written materials allowed.
- Do not write any answers on this questions paper

1. (a) (5 points) Figure 1 depicts an amplifier composed of a cascade of three stages. The amplifier is fed by a signal source with a source resistance of $100\,\text{k}\Omega$ and delivers its output into a load resistance of $100\,\Omega$. The first stage has a relatively high input resistance and a modest gain factor of 10. The second stage has a higher gain factor of 100 but a lower input resistance. Finally, the last, or output, stage has unity gain but a low output resistance. Calculate the overall gain of the amplifier. Express your answer in dB.

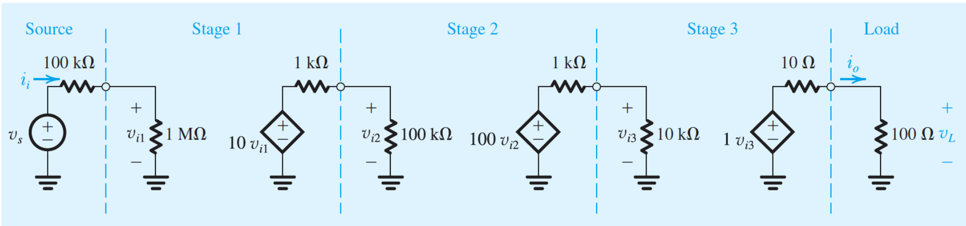


FIGURE 1. Three-stage amplifier

Solution:

- The fraction of the source signal that appears at the the input terminal is given by Equation (1)

$$\frac{v_{i1}}{v_s} = \frac{1\,\text{M}\Omega}{1\,\text{M}\Omega + 100\,\text{k}\Omega} = 0.909V/V \tag{1}$$

- The voltage gain of the first stage is calculated by considering the input resistance of the second stage (Equation (2))

$$A_{v1} \equiv \frac{v_{i2}}{v_{i1}} = 10\frac{10\,\text{k}\Omega}{100\,\text{k}\Omega + 1\,\text{k}\Omega} = 9.9V/V \tag{2}$$

- In the same manners, the voltage gain of the second stage is given by Equation (3)

$$A_{v1} \equiv \frac{v_{i3}}{v_{i2}} = 100\frac{10\,\text{k}\Omega}{10\,\text{k}\Omega + 1\,\text{k}\Omega} = 90.9V/V \tag{3}$$

- The voltage gain of the output stage is given Equation (4)

$$A_{v1} \equiv \frac{v_L}{v_{i3}} = \frac{100\,\Omega}{100\,\Omega + 10\,\Omega} = 0.909V/V \tag{4}$$

- The overall gain is the product of the three gains (Equation (5))

$$\begin{aligned} A_v &= fracv_L v_{i1} = A_{v1}A_{v2}A_{v3} = 818V/V = 818V/V \\ &= 20log(818) = 58.25\,\text{dB} \end{aligned} \tag{5}$$

(b) Figure 2 represents a portion of battery-charger circuit for a battery with a voltage V_B. The sine-wave input $v_S = 12\,\text{V}(rms)$, while the battery voltage varies from 12 V to 14 V from the discharged to fully charged states. The charging-source resistance $R_S = 10\,\Omega$. Assuming that D is an ideal diode, and $R_C = 50\,\Omega$ is a current-controlling resistor established by the designer:

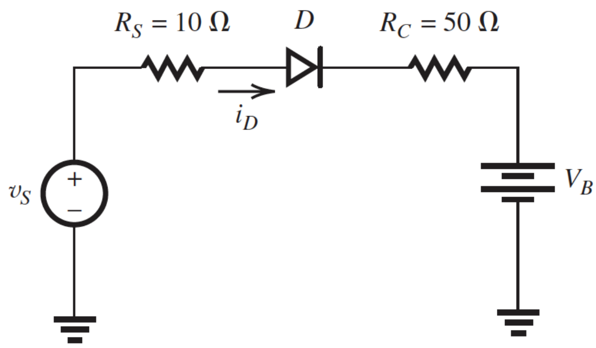
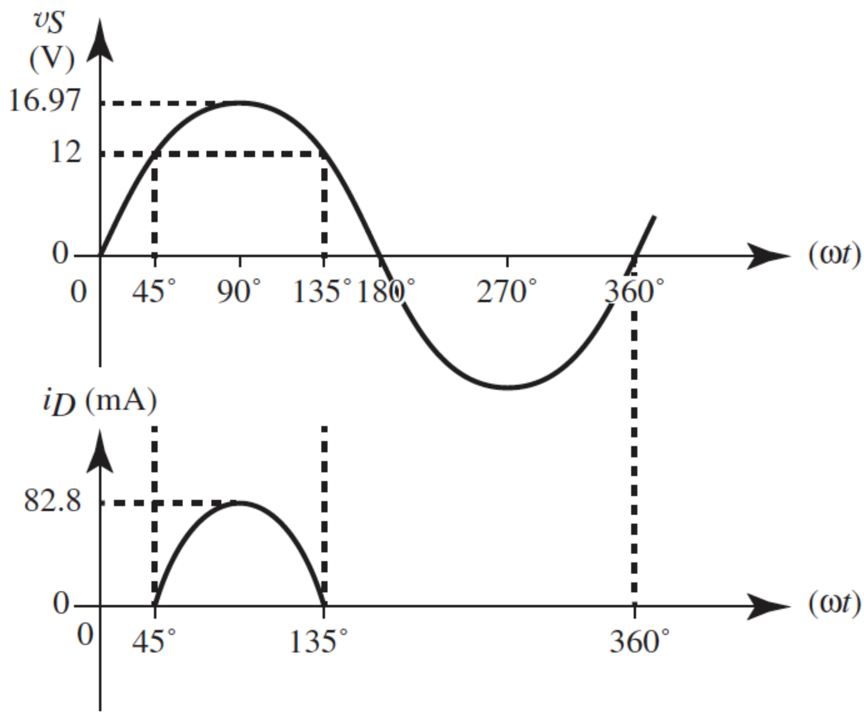


FIGURE 2. Battery-charger circuit

i. (5 points) Sketch and label the voltage waveforms of the voltage accros the diode and the current through the diode for $V_B = 12\,\text{V}$.

Solution: The current and voltages for r $V_B = 12\,\text{V}$ is shown below



Note: To receive the full marks, the student should show:

- Clear units
- Clear labels and their values
- That the peak is at 90 degrees

ii. (5 points) What is the peak diode current?

Solution: For a battery voltage VB and an ideal diode, the diode current is

$$\begin{aligned} i_D &= \frac{v_s - V_B}{R_S + R_C} \\ &= \frac{V_S' sin(\omega t) - V_B}{10\,\Omega + 50\,\Omega} \end{aligned} \tag{6}$$

where $V_S' = \sqrt{2} \times 12V = 16.97V$. Thus, for $V_B = 12V$, the current is given in Equation (7)

$$i_D = \frac{16.97 sin(\omega t)V - 12V}{60\,\Omega} \tag{7}$$

Equation (7) shows that the peak current would be (Equation (8))

$$i_{Dmax} = \frac{16.97V - 12V}{60\,\text{V}} = 82.8\,\text{mA} \tag{8}$$

(c) An NMOS transistor is fabricated in a 0.13 µm CMOS process (i.e., $L_{min} = 0.13$ µm) with $L = 1.5L_{min}$, $W = 1.3$ µm. The process technology is specified to have an oxide layer $t_{ox} = 2.7$ nm, $\mu_n = 400\,\text{cm}^2\,\text{V}^{-1}$ s and $V_{tn} = 0.4V$

i. (6 points) Find the oxide capacitance, C_{ox}, the process transconductance, k_n', and the MOSFET transconductance parameter, k_n. The permittivity of the silicon dioxide, $\epsilon_{ox} = 3.45 \times 10^{-11} F \cdot m^{-1}$

Solution:

$$L = 1.5L_{min} = 1.5 \times 0.13 = 0.195\,\mu\text{m} \tag{9}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = 1.28^{-2} F/m^2 \tag{10}$$

$$\begin{aligned} k_n' &= \mu_n C_{ox} \\ &= 512 \times 10^{-6} A/V^2 \end{aligned} \tag{11}$$

$$\begin{aligned} k_n &= k_n' \frac{W}{L} \\ &= 3413\,\mu\text{A}\,\text{V}^{-2} \end{aligned} \tag{12}$$

ii. (6 points) Find the overdrive voltage V_{OV} and the minimum value of V_{DS} required to operate the transistor in saturation at a current $I_D = 100\,\mu A$. What gate-to-source voltage is required?

Solution: When the MOSFET operates in saturation, the current is given by

$$I_D = \frac{1}{2} k_n V_{OV}^2 \tag{13}$$

Thus,

$$V_{OV} = \sqrt{\frac{I_D}{\frac{1}{2}k_n}} = 0.24V \tag{14}$$

As V_{GS} is reduced, r_{DS} increases, becoming infinite when the channel disappears, which occurs as V_{OV} reaches zero or, correspondingly,

$$V_{GS} = V_{tn} = 0.4V \tag{15}$$

(d) (6 points) For the NMOS transistor in Figure 3, determine the values of R_D and R_S so that the transistor operates at $i_D = 0.4mA$ and $V_D = +0.5V$. The NMOS transistor has $V_t = 0.7V$, $\mu_n C_{ox} = 100\mu A/V^2$, $L = 1\,\mu m$, and $W = 32\,\mu m$. Neglect the channel-length modulation effect (i.e., $\lambda = 0$).

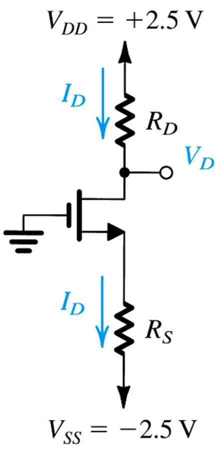


FIGURE 3. NMOS transistor

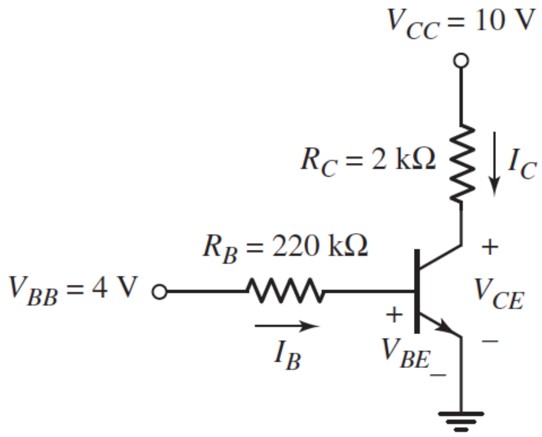


FIGURE 4. Common-emitter BJT circuit

Solution:

- For a V_D voltage, we have

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{2.5 - 0.5}{0.4} = 5\,k\Omega \tag{16}$$

- To calculate R_S we need to know the voltage at the source terminal.
  - Since $V_D = 0.5 > V_G$, the transistor is in the saturation mode. Thus,

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{OV}^2 \quad (17)$$

The overdrive voltage is thus given by

$$V_{OV} = \sqrt{\frac{I_D}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}}} = 0.5V \quad (18)$$

  - It is now possible to calculate V_{GS}

$$V_{GS} = V_t + V_{OV} = 0.7V + 0.5V = 1.2V \quad (19)$$

  - The source resistor is thus given by

$$R_S = \frac{V_G - V_S - V_{SS}}{I_D} = \frac{0 - 1.2 - (-2.5)}{0.4} = 3.25\,\text{k}\Omega \quad (20)$$

(e) For the common-emitter circuit in Figure 4,

i. (5 points) Calculate the base current, collector current, emitter currents, the V_{CE} voltage and the transistor power dissipation. Assume $\beta = 200$ and $V_{BE}(on) = 0.7V$

Solution:

- The base current is found as

$$\begin{aligned} I_B &= \tfrac{V_{BB} - V_{BE}(on)}{R_B} \\ &= \tfrac{4V - 0.7V}{220k} \\ &= 15\,\mu\text{A} \end{aligned} \quad (21)$$

- The collector current is

$$I_C = \beta I_B = 200 \times 15\,\mu\text{A} = 3mA \quad (22)$$

- The emitter current is

$$I_E = (1+\beta)I_B = 3.02mA \quad (23)$$

- The collector-emitter voltage is

$$V_{CE} = V_{CC} - I_C R_C = 4V \tag{24}$$

- The power dissipated is

$$\begin{aligned} P_T &= I_B V_{BE}(on) + I_C V_{CE} \\ &= 0.015 \times 0.7 + 3 \times 4 \\ &= 12mW \end{aligned} \tag{25}$$

ii. (2 points) What is the mode of operation for the BJT in Figure 4? Briefly explain your answer.

Solution: Since $V_{BB} > V_{BE}(on)$ and $V_{CE} > V_{BE}(on)$, the transistor is biased in the forward-active mode.

2. The NMOS transistor in the circuit in Figure 5 has $V_{tn} = 0.5V$, $k'_n = 400\,\mu A\,V^{-2}$, $W/L = 10$ and $\lambda = 0$

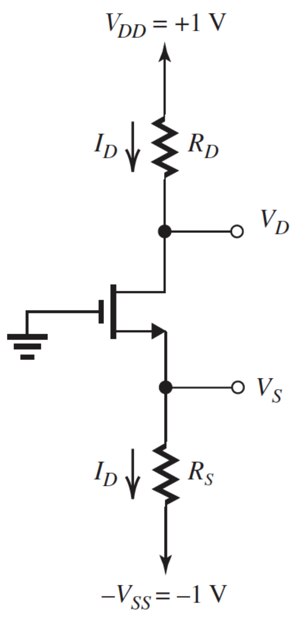


FIGURE 5

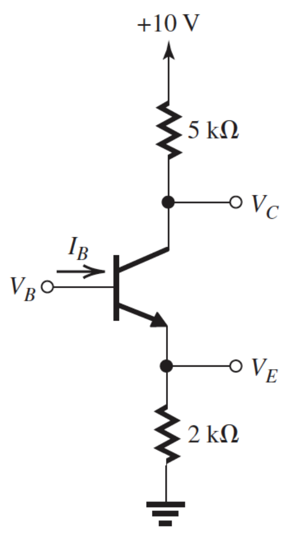


FIGURE 6

(a) (2 points) Find the the transistor's operating mode when $V_D = +0.5V$

Solution: When $V_D = +0.5V$, then the transistor will be in the saturation mode since $V_D > V_G$

(b) (4 points) Find the required values of R_S and R_D to obtain $i_D = 180\,\mu A$ and $V_D = +0.5V$. Also, find the voltage V_S that results

Solution:

- As shown in the previous solution, for $V_D = 0.5V$, the transistor will be in the saturation mode. Hence,

$$I_D = \frac{1}{2} k_n' \left(\frac{W}{L} \right) V_{OV}^2 \tag{26}$$

- Solving Equation (26) given the required value of V_{OV}

$$180 = \frac{1}{2} \times 400 \times 10 V_{OV}^2 \Rightarrow V_{OV} = 0.3V \tag{27}$$

- V_{GS} is calculated as shown in Equation (28)

$$V_{GS} = V_{tm} + V_{OV} = 0.5 + 0.3 = 0.8V \tag{28}$$

- Consequently,

$$V_S = V_G - V_{GS} = 0 - 0.8 = -0.8V \tag{29}$$

- And the required value for R_S is given as

$$\begin{aligned} R_S &= \tfrac{V_S - (-V_S S)}{I_D} \\ &= \tfrac{-08 - (-1)}{180\,\mu A} \\ &= 1.11\,k\Omega \end{aligned} \tag{30}$$

- The value of the R_D resistor is given as

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{1V - 0.5V}{0.18mA} = 2.78\,k\Omega \tag{31}$$

(c) (4 points) What is the largest value to which R_D can be increased while the transistor remains in the saturation mode?

Solution:

- As R_D is is increased, V_D decreases (Equation (32))

$$\begin{aligned} V_D &= 1 - I_D R_D \\ &= C \\ &= D \end{aligned} \tag{32}$$

- Eventually, V_D falls below VG by V_{tn} at which point the transistor leaves the saturation region and enters the triode region. This occurs at

$$V_D = V_G - V_{tn} = -0.5V \tag{33}$$

- The corresponding value of R_D is given by

$$-0.5 = V - 0.18R_D \Rightarrow R_D = 8.3\,\mathrm{k}\Omega \tag{34}$$

3. The BJT in Figure 6 has $\beta = 100$, $V_{CESat} = 0.3V$ and $V_B(on) = 0.7V$. Find V_E, V_C and I_B and the transistor's mode of operation:

(a) (3 points) When $V_B = 0V$

Solution: In this case, the transistor is in cut-off mode. Thus,

- $i_B = 0$
- $V_E = V_B = 0$
- $V_C = 10V$

(b) (3 points) When $V_B = 3V$

Solution: In this case, the transistor is in the active mode

- $V_E = V_B - V_{on} = 3 - 0.7 = 2.3V$
- $I_E = \frac{V_E}{2k} = \frac{2.3}{2k} = 1.15mA$
- $I_C = \alpha I_E = 0.99 \times 1.15 = 1.14mA$
- $I_B = I_E - I_C = 0.01mA$
- $V_C = 10V - I_C R_C = 4.3V$

(c) (4 points) When $V_B = 5V$

Solution: If we apply the same approach as in (b) above (and assume that the transistor is in active mode), we would notice that $I_C < 0$, which is not possible. Thus, the transistor must be in active mode. In this case:

- $V_E = 4.3V$
- $I_E = 4.3/2 = 2.15mA$
- $V_C = V_E + V_{CESat} = 4.3 + 0.3V = 4.6V$
- $I_C = \frac{10V - 4.6V}{5} = 1.08mA$
- $I_B = I_E - I_C = 1.07mA$