DEPARTMETN OF ELECTRICAL & ELECTRONICS ENGINEERING

END OF SEMESTER EXAMINATION -ACADEMIC YEAR 2020-2021

TRIMESTER I

GROUP: Y2 EPE

MODULE: EPE2165—ANALOG ELECTRONICS

DATE: 14/09/2021

TIME: 2 hours

MAX POINTS = 50 POINTS

INSTRUCTIONS

- You have 2 hours to complete the exam. Be a smart test taker: if you get stuck on one problem go on to the next.
- This exam paper comprises 3 pages, excluding the title page. Please check that you have received all of them.
- This exam paper contains 3 questions. Answer only 2 questions as follows
    - QUESTION # 1 is COMPULSORY
    - Chose ONE (1) question from questions 2 and 3
    - If a candidate answers more than two questions, at the sole discretion of the grader, only two questions will be graded.
- Keep your answers short and to the point. Longer is not necessarily better as the number of written words is NOT a grading criterion and, in some case, longer answers may even make your answer abstruse.
- Write legibly. If the grader cannot read it, you will not get credit for it.
- Write all your answers in the answer booklet provided
- Do not forget to write your Registration Number
- No written materials allowed.
- Do not write any answers on this questions paper

1. (a) (5 points) Figure 1 depicts an amplifier composed of a cascade of three stages. The amplifier is fed by a signal source with a source resistance of 100 kΩ and delivers its output into a load resistance of 100 Ω. The first stage has a relatively high input resistance and a modest gain factor of 10. The second stage has a higher gain factor of 100 but a lower input resistance. Finally, the last, or output, stage has unity gain but a low output resistance. Calculate the overall gain of the amplifier. Express your answer in dB.

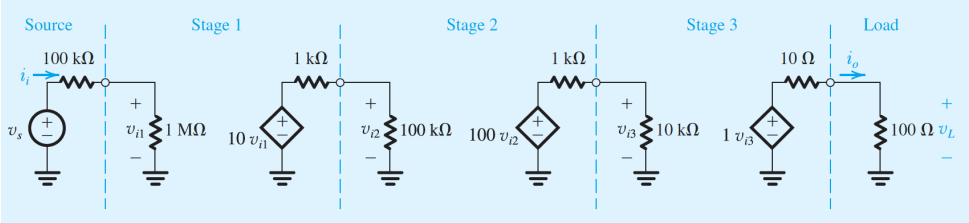

FIGURE 1. Three-stage amplifier

(b) Figure 2 represents a portion of battery-charger circuit for a battery with a voltage V_B. The sine-wave input $v_S = 12\,\text{V}(rms)$, while the battery voltage varies from 12 V to 14 V from the discharged to fully charged states. The charging-source resistance $R_S = 10\,\Omega$. Assuming that D is an ideal diode, and $R_C = 50\,\Omega$ is a current-controlling resistor established by the designer:

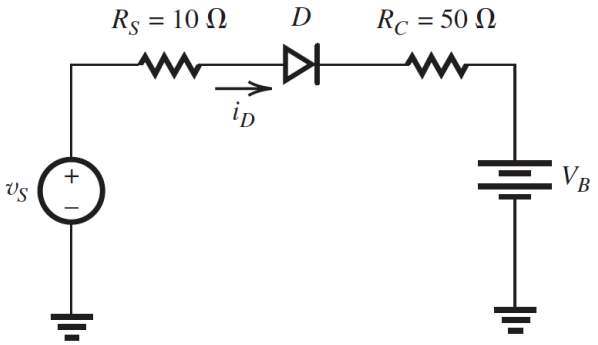

FIGURE 2. Battery-charger circuit

i. (5 points) Sketch and label the voltage waveforms of the voltage accros the diode and the current through the diode for $V_B = 12\,\text{V}$.

ii. (5 points) What is the peak diode current?

(c) An NMOS transistor is fabricated in a 0.13 µm CMOS process (i.e., $L_{min} = 0.13\,\mu\text{m}$) with $L = 1.5L_{min}$, $W = 1.3\,\mu\text{m}$. The process technology is specified to have an oxide layer $t_{ox} = 2.7\,\text{nm}$, $\mu_n = 400\,\text{cm}^2\,\text{V}^{-1}\,\text{s}$ and $V_{tn} = 0.4V$

i. (6 points) Find the oxide capacitance, C_{ox}, the process transconductance, k'_n, and the MOSFET transconductance parameter, k_n. The permittivity of the silicon dioxide, $\epsilon_{ox} = 3.45 \times 10^{-11} F \cdot m^{-1}$

ii. (6 points) Find the overdrive voltage V_{OV} and the minimum value of V_{DS} required to operate the transistor in saturation at a current $I_D = 100\,\mu A$. What gate-to-source voltage is required?

(d) (6 points) For the NMOS transistor in Figure 3, determine the values of R_D and R_S so that the transistor operates at $i_D = 0.4mA$ and $V_D = +0.5V$. The NMOS transistor has $V_t = 0.7V$, $\mu_n C_{ox} = 100\mu A/V^2$, $L = 1\,\mu m$, and $W = 32\,\mu m$. Neglect the channel-length modulation effect (i.e., $\lambda = 0$).

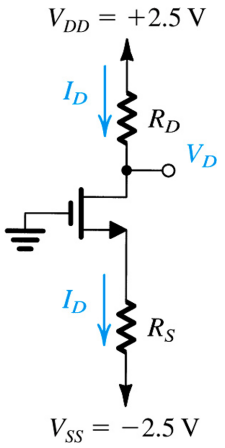

FIGURE 3. NMOS transistor

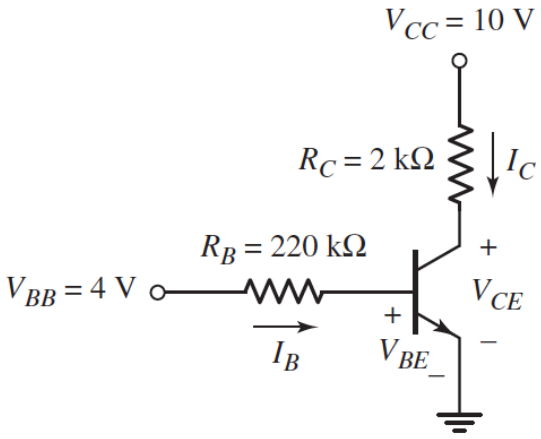

FIGURE 4. Common-emitter BJT circuit

(e) For the common-emitter circuit in Figure 4,

i. (5 points) Calculate the base current, collector current, emitter currents, the V_{CE} voltage and the transistor power dissipation. Assume $\beta = 200$ and $V_{BE}(on) = 0.7V$

ii. (2 points) What is the mode of operation for the BJT in Figure 4? Briefly explain your answer.

2. The NMOS transistor in the circuit in Figure 5 has $V_{tn} = 0.5V$, $k'_n = 400\,\mu A\,V^{-2}$, $W/L = 10$ and $\lambda = 0$

(a) (2 points) Find the the transistor's operating mode when $V_D = +0.5V$

(b) (4 points) Find the required values of R_S and R_D to obtain $i_D = 180\,\mu A$ and $V_D = +0.5V$. Also, find the voltage V_S that results

(c) (4 points) What is the largest value to which R_D can be increased while the transistor remains in the saturation mode?

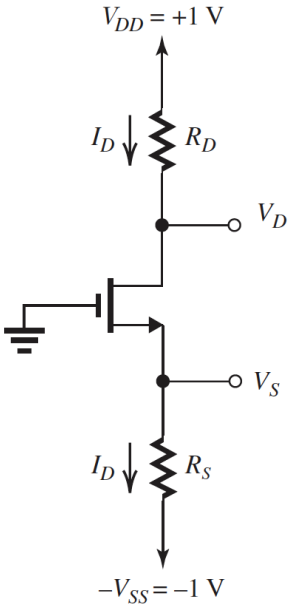

FIGURE 5

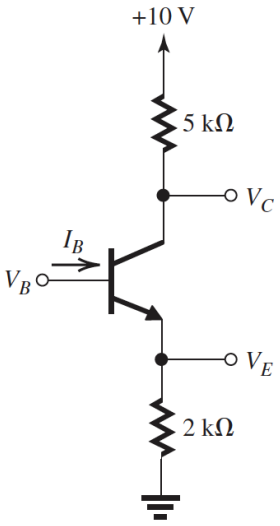

FIGURE 6

3. The BJT in Figure 6 has $\beta = 100$, $V_{CESat} = 0.3V$ and $V_B(on) = 0.7V$. Find V_E, V_C and I_B and the transistor's mode of operation:

   (a) (3 points) When $V_B = 0V$

   (b) (3 points) When $V_B = 3V$

   (c) (4 points) When $V_B = 5V$