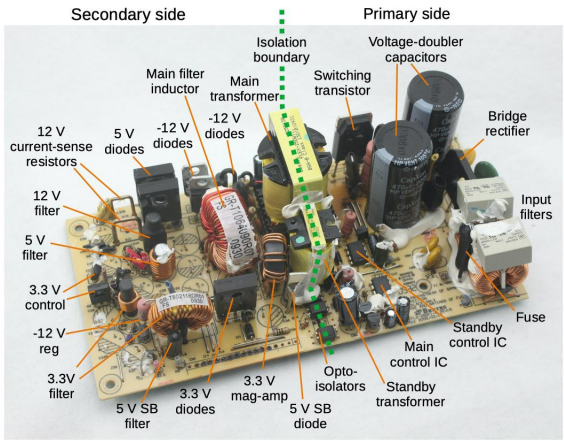


Current–Voltage Characteristics

Kizito NKURIKIYEYEZU,

Circuit Symbol

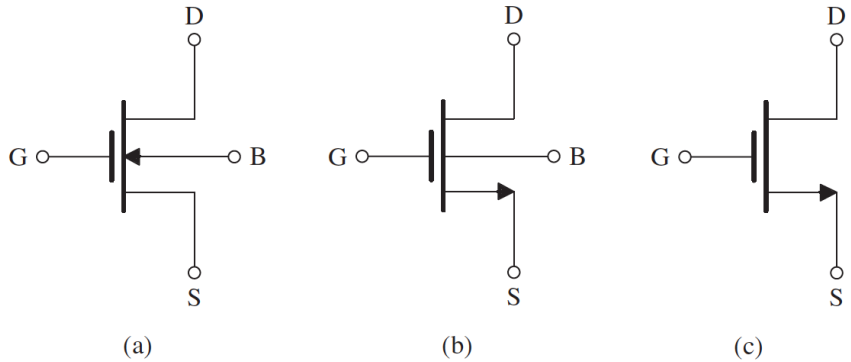


FIG 1. Common MOSFET circuit symbols
(a) Circuit symbol for the n-channel enhancement-type MOSFET. (b) Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., n channel). (c) Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

Circuit Symbol

Fig. 2 shows the circuit symbol for the n-channel enhancement-type MOSFET

- The larger vertical line represent the channel region
- The small line represents the gate
- The two lines are separated by a white space —to indicate the fact that the gate electrode is insulated from the body of the device.
- The arrowhead also indicates the polarity of the

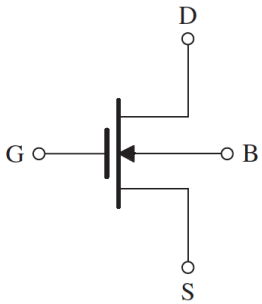


FIG 2. Symbol 1

Circuit Symbol

Fig. 3 shows the circuit symbol for the n-channel enhancement-type MOSFET

- The arrowhead is placed on the source terminal, thus distinguishing it from the drain terminal.
- The arrowhead is a reminder that normally $V_D > V_S$, thus the current flows from the drain to the source.

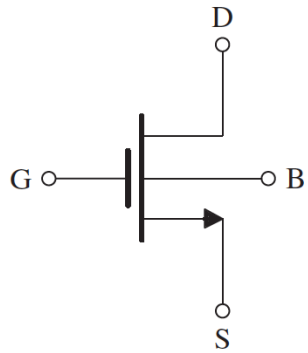


FIG 3. Symbol 2

Circuit Symbol

Fig. 4 shows the circuit symbol for the n-channel enhancement-type MOSFET. There are only three terminals to remind that in most applications:

- The body is connected to the source
- Or the body is connected to the lowest voltage
- In all cases, the body is not changing, so it can be ignored since its effect on circuit operation is not important,

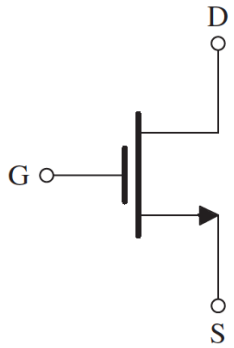


FIG 4. Symbol 3

The i_D vs v_{DS} characteristics for an enhancement-type NMOS transistor

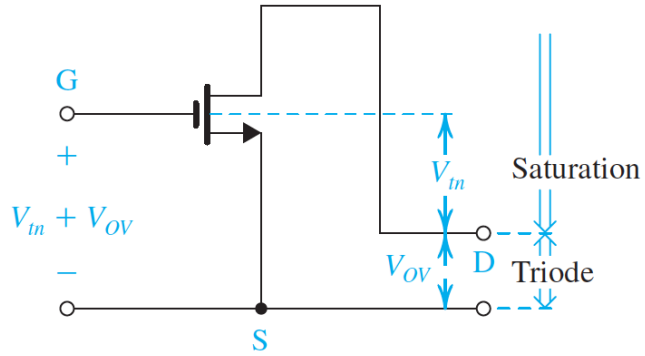


FIG 5. The relative levels of the terminal voltages of the enhancement NMOS transistor for operation in the triode region and in the saturation region. Note that the operation mode depend on the drain-source voltage

Summary: Regions of Operation of a MOSFET Transistor

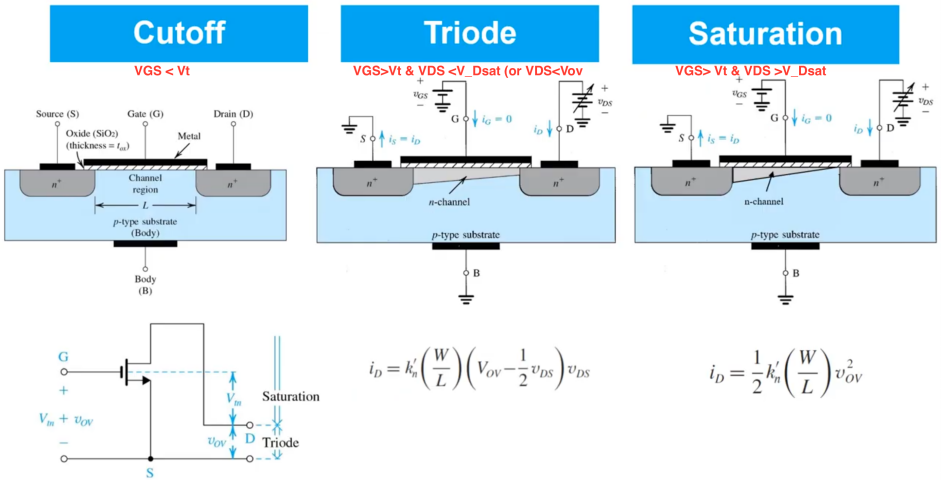
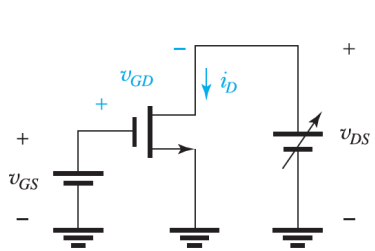
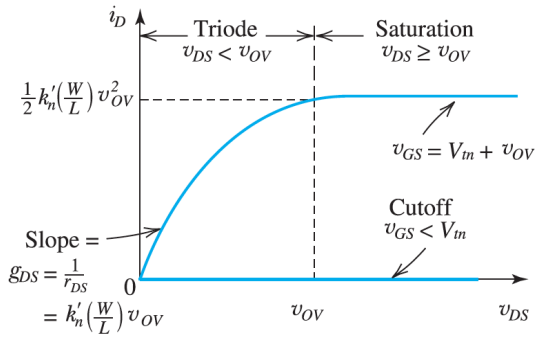


FIG 6

Summary: Regions of Operation of an NMOS Transistor

- $v_{GS} < V_t$—no channel. The transistor is in the cut-off mode. $i_D = 0$





[0] In the triode, i_D is controlled by three terminals (hence the name triode), unlike in the saturation mode, where the transistor's operation is controlled by two terminals

Summary: Regions of Operation of an NMOS Transistor

- $v_{GS} = V_{tn} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched off at the drain end;

Triode Region

Continuous channel, obtained by:

$$v_{GD} > V_{tn}$$

or equivalently:

$$v_{DS} < v_{OV}$$

Then,

$$i_D = k_n' \left(\frac{W}{L}\right)\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

or equivalently,

$$i_D = k_n' \left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{GD} \leq V_{tn}$$

or equivalently:

$$v_{DS} \geq v_{OV}$$

Then

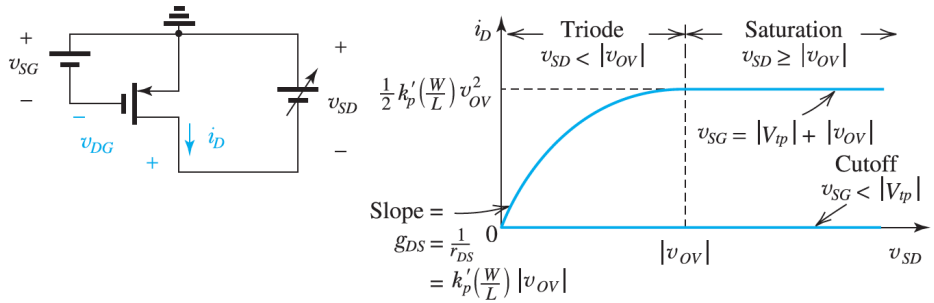
$$i_D = \frac{1}{2}k_n' \left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

or equivalently,

$$i_D = \frac{1}{2}k_n' \left(\frac{W}{L}\right)v_{OV}^2$$

Summary: Regions of Operation of an PMOS Transistor

- $v_{SG} < |V_{tp}|$—no channel, transistor is off and $i_D = 0$



Summary: Regions of Operation of an PMOS Transistor

- $v_{SG} = |V_{tp}| + |v_{OV}|$: a channel is induced; transistor operates in the triode region or in the saturation region depending on whether the channel is continuous or pinched off at the drain end;

Triode Region

Continuous channel, obtained by:

$$v_{DG} > |V_{tp}|$$

or equivalently

$$v_{SD} < |v_{OV}|$$

Then

$$i_D = k_p' \left(\frac{W}{L}\right)\left[(v_{SG} - |V_{tp}|)v_{SD} - \frac{1}{2}v_{SD}^2\right]$$

or equivalently

$$i_D = k_p' \left(\frac{W}{L}\right)\left(|v_{OV}| - \frac{1}{2}v_{SD}\right)v_{SD}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{DG} \leq |V_{tp}|$$

or equivalently

$$v_{SD} \geq |v_{OV}|$$

Then

$$i_D = \frac{1}{2}k_p' \left(\frac{W}{L}\right)(v_{SG} - |V_{tp}|)^2$$

or equivalently

$$i_D = \frac{1}{2}k_p' \left(\frac{W}{L}\right)v_{OV}^2$$

FIG 7

The i_D vs v_{DS} characteristics for an enhancement-type NMOS transistor

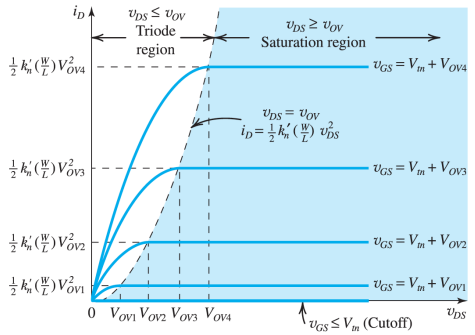


FIG 8. The i_D vsv_{DS} characteristics for an enhancement-type NMOS transistor Note that each graph is obtained by setting v_{GS} above V_{tn} by a specific value of overdrive voltage, denoted $VOV1$, $VOV2$,$VOV3$ and $VOV4$. This in turn is the value of v_{DS} at which the corresponding graph saturates, and the value of the resulting saturation current is directly determined by the value of v_{OV} , namely, $1/2k_nV_{OV1}^2$, $1/2k_nV_{OV2}^2$, etc

The i_D vs v_{GS} characteristic

- As shown by Fig. 8, in saturation the drain current is constant determined by v_{GS} (or v_{OV}) and is independent of v_{DS}.
- The MOSFET operates as a voltage-controlled current source with the control relationship described by Equation (1)

$$i_D = \frac{1}{2}k'_n\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2 = \frac{1}{2}k'_n\left(\frac{W}{L}\right)v_{OV}^2 \quad (1)$$

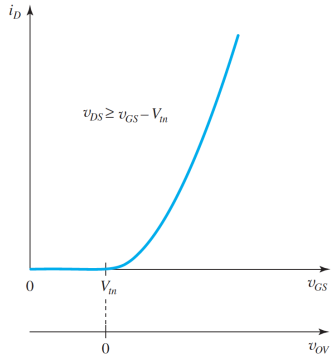


FIG 9. The i_D vs v_{GS} characteristic in the saturation region. The i_D vs v_{GS} characteristic can be obtained by simply relabeling the horizontal axis, that is, shifting the origin to the point $v_{GS} = V_{tn}$

Equivalent circuit for a MOSFET

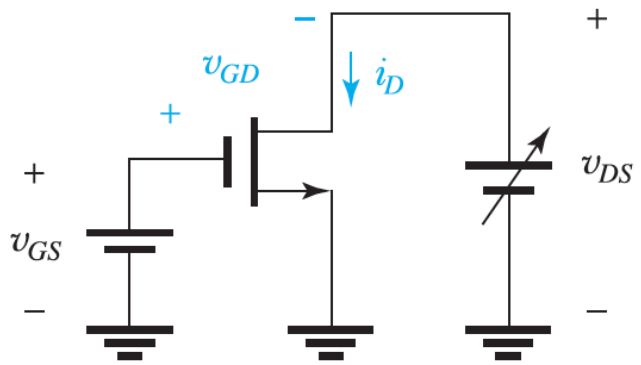


FIG 10. MOSFET circuit

Equivalent circuit for a MOSFET

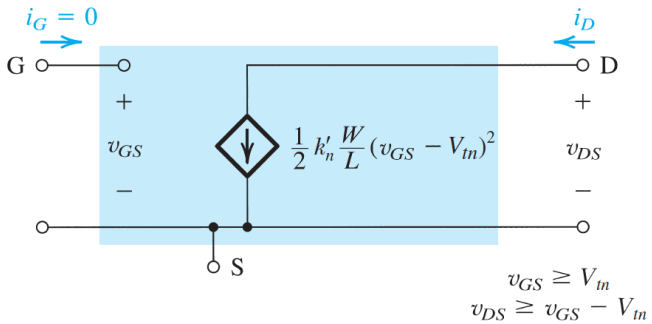


FIG 11. Equivalent Circuit for MOSFET in saturation
The Figure represents the square law model of the circuit in Fig. 10. It is a large-signal, equivalent-circuit model of an n-channel MOSFET operating in the saturation region. Note that the current source is ideal, with an infinite output resistance representing the independence, in saturation, of i_D from v_{DS}. Also, note that the gate is disconnected since it would be insulated by the oxide layer.