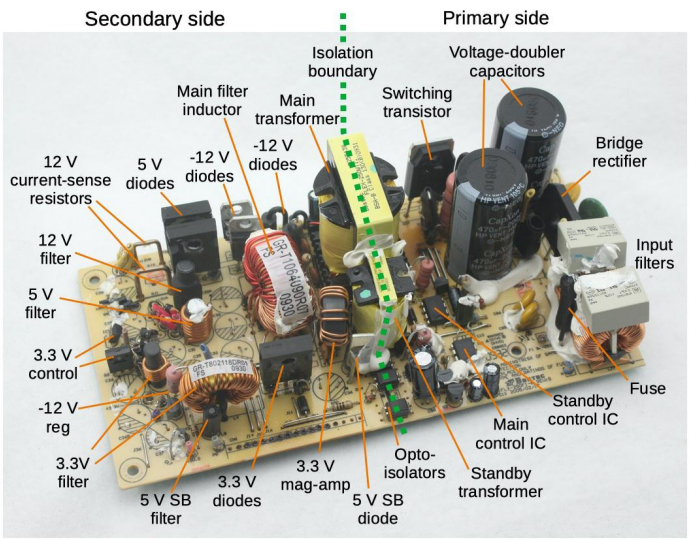

MOSFETs

Kizito NKURIKIYEYEZU, Ph.D.

Introduction

- Transistors are three-terminal devices —unlike diodes, which have only two
- The basic usage of a transistor is the ability to use the voltage between two terminals to control the current flowing in the third terminal
- They are more useful because they present multitude of applications: signal amplification, digital logic, memory, etc. . .
- There are two major types of three-terminal semiconductor devices:
  - BJT—bipolar junction transistor
  - MOSFET—metal oxide-semiconductor field-effect transistor
- MOSFETs are considered preferable to BJT technology for many applications and are much widely used because:
  - size (smaller)
  - ease of manufacture
  - lesser power utilization
  - backbone of very large scale integration (VLSI)
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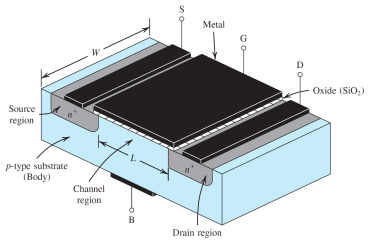
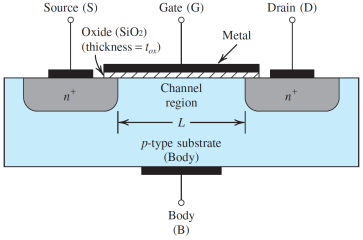
- layer of SiO_2 separates source and drain
- metal, placed on top of SiO_2, forms gate electrode
- Four terminals: the gate(G), the source (S), the drain (D) and the Body (B).



(a) perspective view



(b) cross section

FIG 1. Physical structure of the enhancement-type NMOS transistor.
Typically $L = 0.03\,\mu m$ to $1\,\mu m$, $W = 0.05\,\mu m$ to $100\,\mu m$, and the thickness of the oxide layer (tox) is in the range of 1 to 10 nm.

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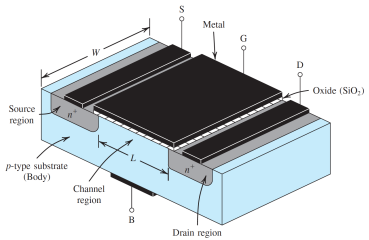

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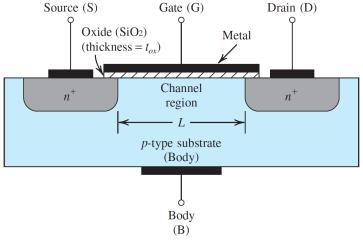

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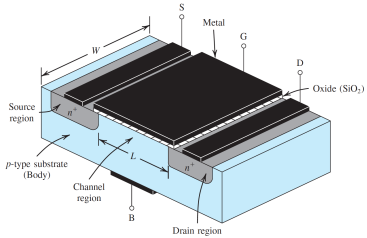

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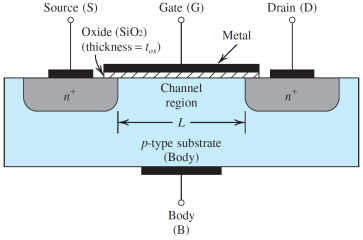

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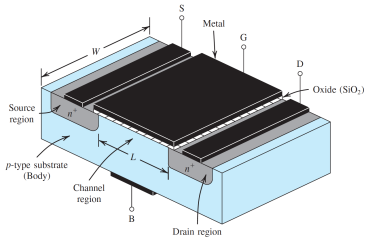

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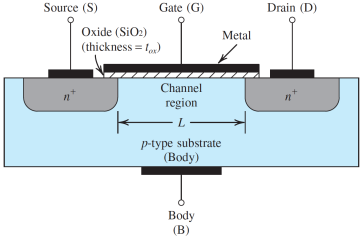

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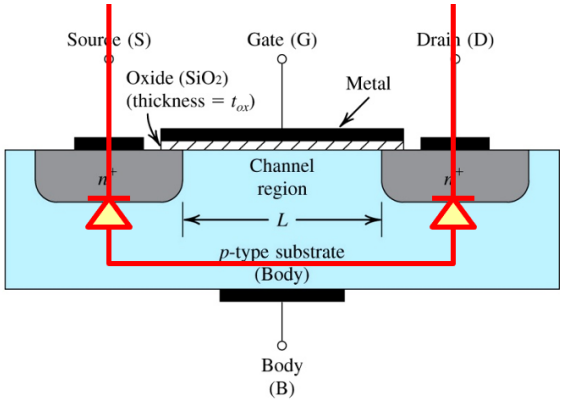
Operations with zero gate voltage

- With zero voltage applied to gate, two back-to-back diodes exist in series between drain and source.
- These diodes prevent current conduction from drain to source when a voltage v_{DS} is applied.
- In short, the path between drain and source has a very high resistance (of the order of 10 TΩ.



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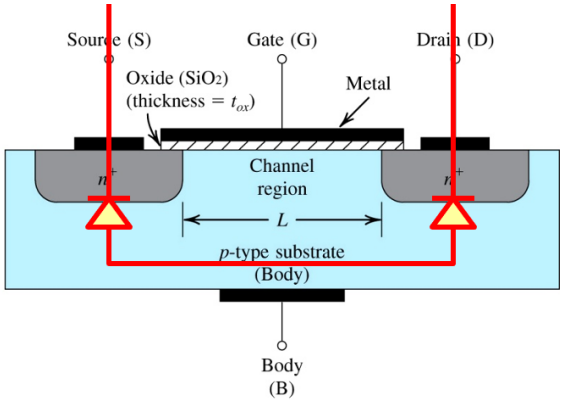

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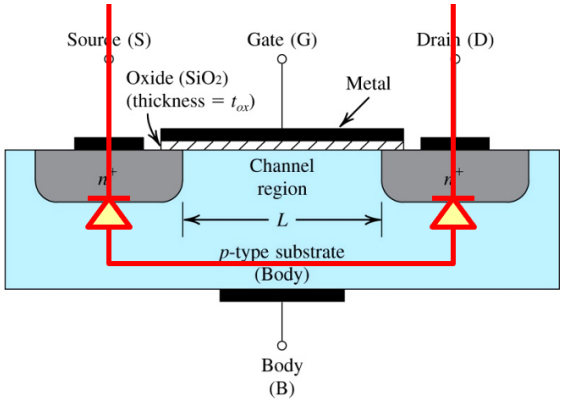


Creating a channel for current flow

What would happen if (1) the source and drain are grounded and (2) a positive voltage is applied to gate ?

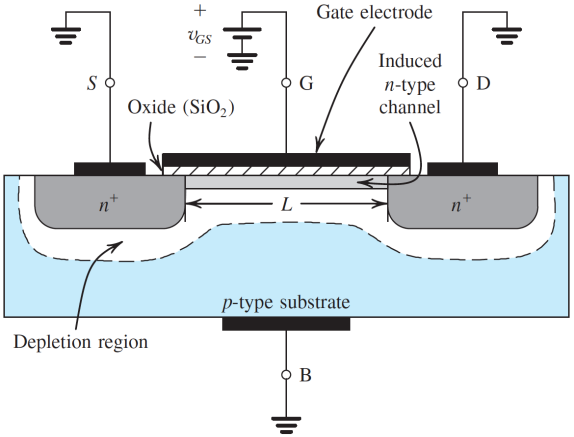
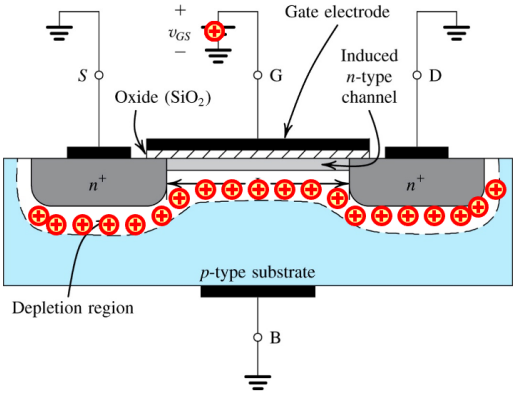


FIG 2. The enhancement-type NMOS transistor with a positive voltage applied to the gate. An n-channel is induced at the top of the substrate beneath the gate.

Creating a channel for current flow

- **Step 1**—v_{GS} is applied to the gate terminal, causing a positive build up of positive charge along metal electrode.
- **Step 2**—This "build up" causes free holes to be repelled from region of p-type substrate under gate.



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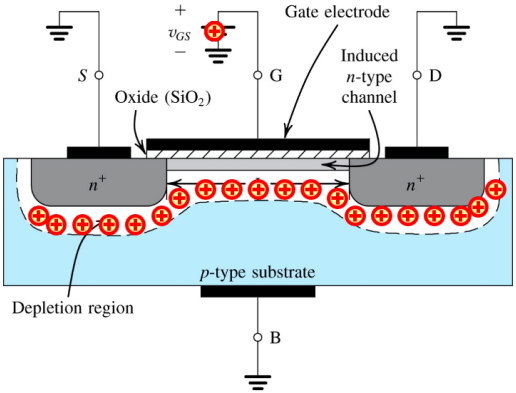

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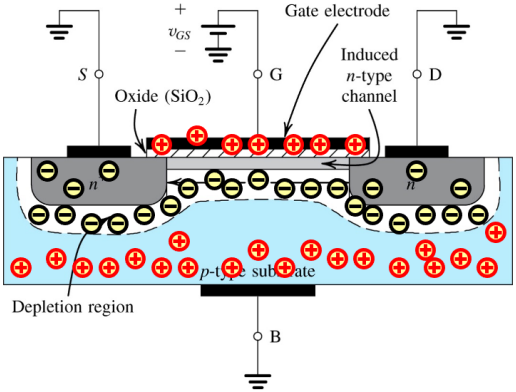

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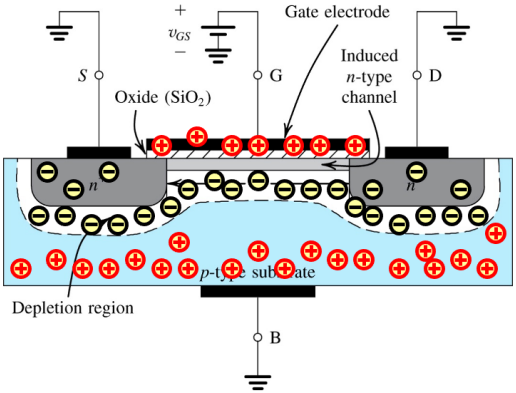

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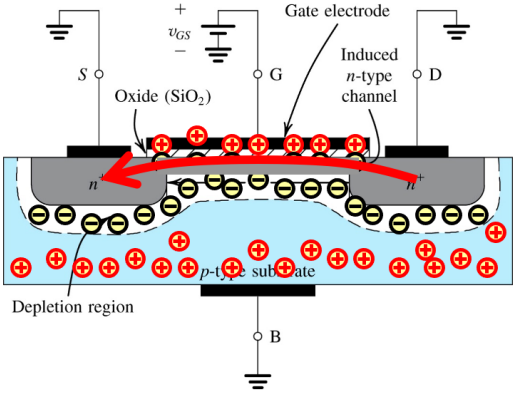
Creating a channel for current flow

- **Step 5**—Once a sufficient number of these electrons accumulate, an n-region is created and connects the source and drain regions
- **Step 6**—This provides path for current flow between D and S.
- **Note:** This induced channel is also known as an inversion layer



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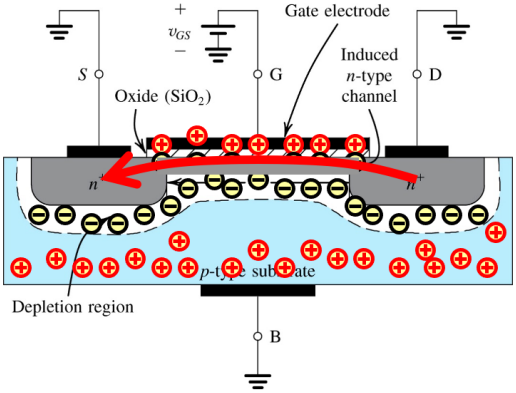

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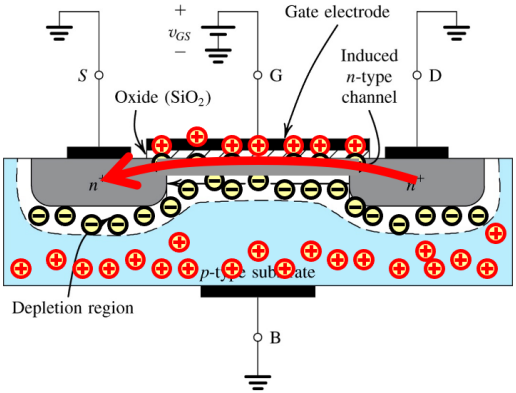

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- threshold voltage Vt[1] – is the minimum value of v_{GS} required to form a conducting channel between drain and source and is between 0.3 and 0.6V[2]
- field-effect —when positive v_{GS} is applied, an electric field develops between the gate electrode and induced n-channel – the conductivity of this channel is affected by the strength of field. The SiO_2 layer acts as dielectric
- The difference between v_{GS} applied and V_t is termed the effective voltage or the overdrive voltage and is the quantity that determines the charge in the channel. It is noted as shown in Equation (1)

$$v_{GS} - Vt \equiv v_{ov} \tag{1}$$

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Creating a channel for current flow

- A conducting channel forms a parallel plate capacitor with the gate
- The charge Q created in the charge is given by Equation (2) and Equation (3)

$$Q = CV \tag{2}$$

$$|Q| = C_g \cdot v_{OV} \tag{3}$$

Where the gate capacitor is given by Equation (4)

$$C_g = C_{ox} WL \tag{4}$$

Where:

C_{ox} is the capacitance per unit are
WL is the area of the electrode

Creating a channel for current flow

- Since the parallel plate capacitor is given by expressed by the area A and the distance d between the plates Equation (5)

$$C = \frac{\epsilon A}{d} \tag{5}$$

- Then, the oxide capacitance (Cox) (i.e., the capacitance of the parallel plate capacitor per unit gate area (F/m^2)) is given by

$$C_{ox} = \epsilon_{ox}/t_{ox} \tag{6}$$

where:

ϵ_{ox} is the permittivity of the silicon dioxide $\epsilon_{ox} = 3.45 \times 10^{-11} F/m$
t_{ox}= is the thickness of the silicon layer SiO_2

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- As v_{ov} grows, so does the depth of the n-channel as well as its conductivity.

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- As v_{ov} grows, so does the depth of the n-channel as well as its conductivity.

Creating a channel for current flow

- Since the parallel plate capacitor is given by expressed by the area A and the distance d between the plates Equation (5)

$$C = \frac{\epsilon A}{d} \tag{5}$$

- Then, the oxide capacitance (Cox) (i.e., the capacitance of the parallel plate capacitor per unit gate area (F/m^2)) is given by

$$C_{ox} = \epsilon_{ox}/t_{ox} \tag{6}$$

where:

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Small v_{DS} Model

Small v_{DS} Model for MOSFET

What is the current i_D For small values of v_{DS} (i.e., 50 mV or so)?

- The charge of the parallel plate capacitor between the gate and the channel is given by Equation (8)

$$Q = CV \tag{7}$$

$$|Q| = C_{ox} W L v_{OV} \tag{8}$$

- The charge per unit length Q_n is then given by Equation (9)

$$Q_n = \frac{|Q|}{L} = C_{ox} W L v_{OV} \tag{9}$$

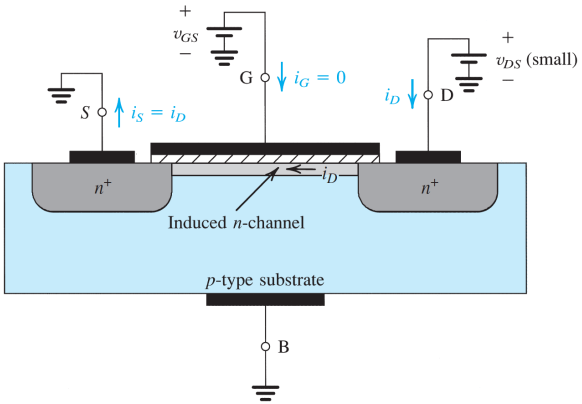

FIG 6. An NMOS transistor with $v > V_t$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to $v_{GS} - Vt$, and thus i_D is proportional to $(v_{GS} - V_t)v_{DS}$.

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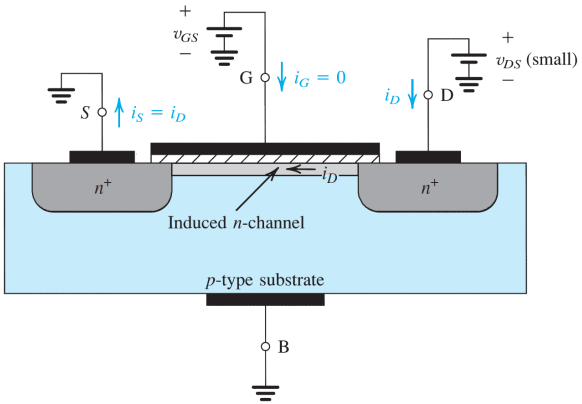

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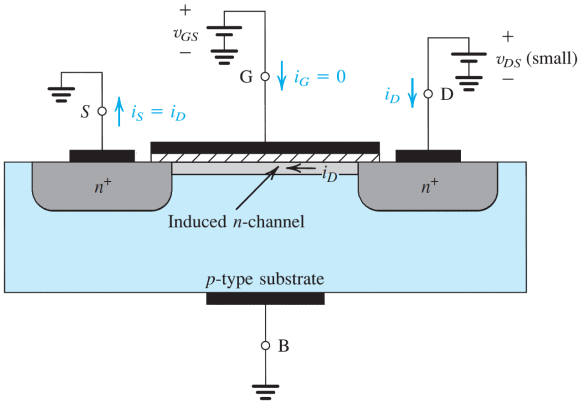
Small v_{DS} Model for MOSFET

- Then the electric field along the channel is given by Equation (10)

$$|E| = \frac{v_{DS}}{L} \tag{10}$$

- The drift velocity of the electrons is given by Equation (11)

$$v_{drift} = \mu_n |E| = \mu_n \frac{v_{DS}}{L} \tag{11}$$



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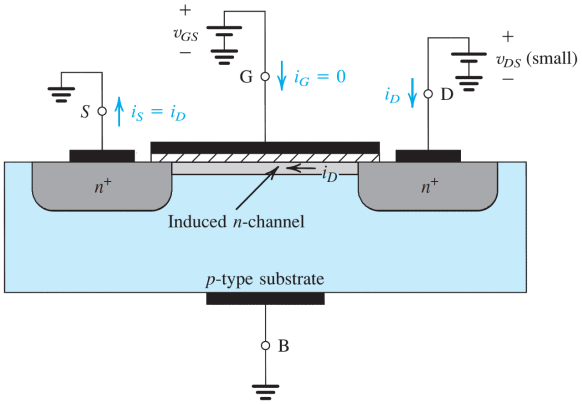

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Small v_{DS} Model for MOSFET

- For small v_{DS}, we can assume that the voltage between the gate and various points along the channel is equal to v_{GS}. i_D is given by Equation (12)[2]

$$\begin{aligned} i_D &= Q_n v_{drift} \\ &= C_{ox} W v_{OV} \mu_n \frac{v_{DS}}{L} \\ &= \left[\mu_n C_{ox} \left(\frac{W}{L}\right) v_{ov}\right] v_{DS} \\ &= \left[\mu_n C_{ox} \left(\frac{W}{L}\right) (v_{GS} - V_t)\right] v_{DS} \end{aligned} \tag{12}$$

- The conductance is given by Equation (13)

$$\begin{aligned} g_{DS} &= \mu_n C_{ox} \left(\frac{W}{L}\right) v_{OV} \\ &= \mu_n C_{ox} \left(\frac{W}{L}\right) (v_{GS} - V_t) \end{aligned} \tag{13}$$

[2] See details in the textbook on page 253

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Small v_{DS} Model for MOSFET

- The factor $k_n' = \mu_n C_{ox}$ is called the process transconductance and is affected by the type of manufacturing process
- The ratio of the width W to the length L (i.e., W/L) affects the conductance. For example, in the recent 5nm lithography technology process, the channel length L cannot be smaller than 5nm.
- A MOSFET transconductance parameter is given by

$$k_n = k_n' \frac{W}{L} = \mu_n C_{ox} \frac{W}{L} \tag{14}$$

- The conductance depends on v_{GS}

$$\begin{aligned} r_{DS} &= 1/g_{DS} \\ &= 1/\mu_n C_{ox}(W/L) v_{OV} \\ &= \frac{1}{\mu_n C_{ox}(W/L)(v_{GS} - V_t)} \end{aligned} \tag{15}$$

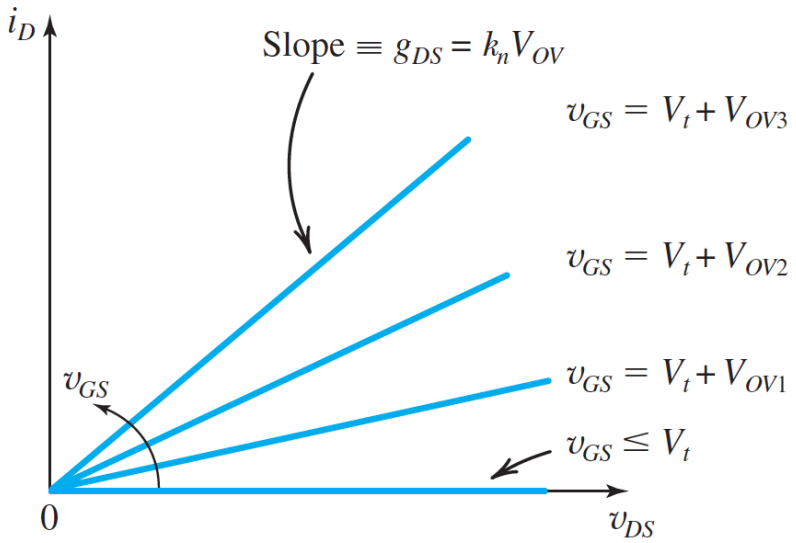

FIG 8. MOSFET operations for various values of v_{GS}
A MOSFET is a voltage-controlled resistance. The slope of the curve which is g_{DS} is dependent on v_{GS} since $V_{OV} = v_{GS} - V_t$. When the voltage applied between drain and source, v_{DS}, is kept small, the device operates as a linear resistance whose value is controlled by v_{GS}.

Large v_{DS} Model

Large v_{DS} Model of a MOSFET

- Let's assume v_{OV} is constant. In this case, as v_{DS} increases, the induced channel width will be different.
- Different v_{GS} will draw different amount of n carrier into the channel creating a non-uniform depth of the channel as shown in Fig. 9
- The channel depth is proportional to v_{GS} at the source end or

$$v_{GS} = V_t + V_{OV} \qquad (16)$$

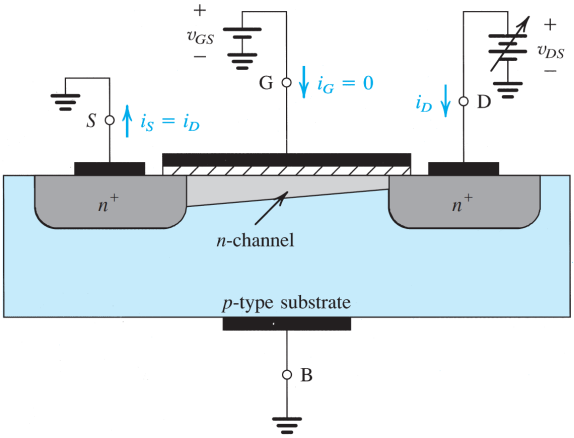

FIG 9. Operation of an NMOS transistor as *vDS* is increased. Note that an unequal channel depth is induced when a larger v_{DS} is applied across the transistor giving rise to non-uniform channel depth

Large v_{DS} Model of a MOSFET

- The channel depth is proportional to v_{GD} at the drain end or

$$v_{GD} = V_t + V_{OV} - vDS \qquad (17)$$

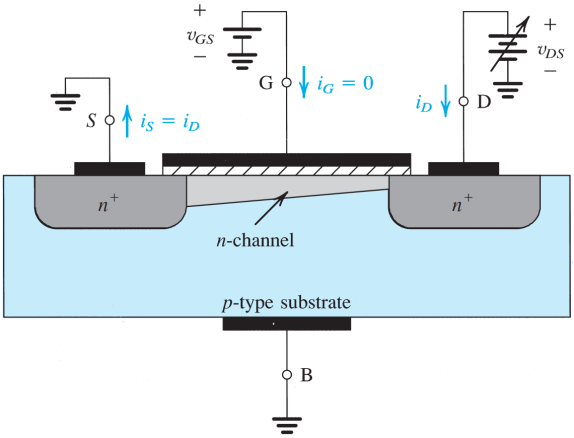

FIG 10. Operation of an NMOS transistor as v_{DS} is increased. Note that an unequal channel depth is induced when a larger v_{DS} is applied across the transistor giving rise to non-uniform channel depth

Non-linearity explanation

- When v_{DS} increases beyond "small values", the relationship between i_D and v_{DS} ceases to be linear.
- Explanation:
  - **step1** Assume that v_{GS} is held constant at value greater than V_t.
  - **step2** Also assume that v_{DS} is applied and appears as voltage drop across n-channel.
  - **step3** Note that voltage decreases from v_{GS} at the source end of channel to v_{GD} at drain end

$$\begin{aligned} v_{GD} &= v_{GS} - v_{DS} \\ &= V_t + v_{OV} - v_{DS} \end{aligned} \tag{18}$$

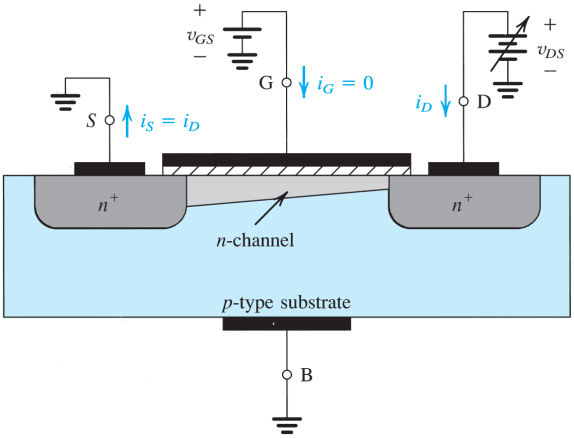

FIG 11. Operation of an NMOS transistor as v_{DS} is increased. Note the unequal channel depth due to a larger v_{DS} is applied across the transistor giving rise to non-uniform channel depth.

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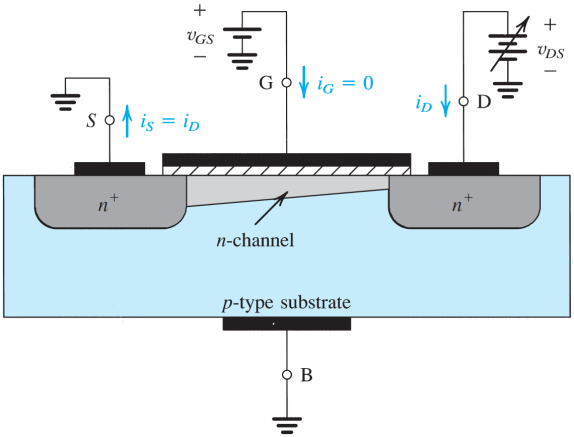

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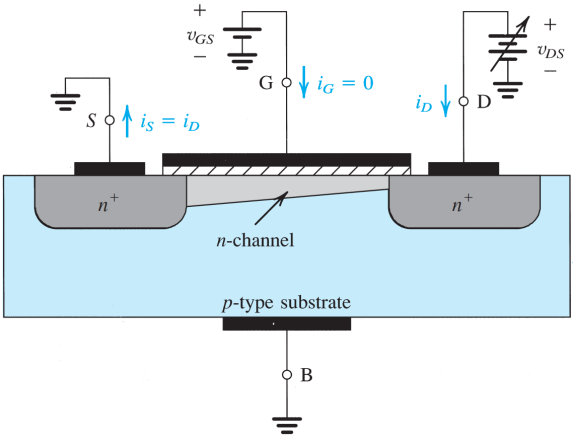

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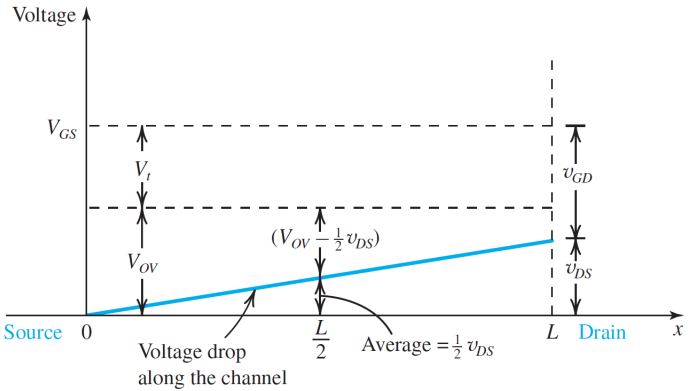
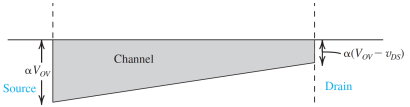


(a) MOSFET with $v_{GS} = V_t + V_{OV}$



(b) Channel shape for MOSFET in Fig. 12a

FIG 12. Linear proportionality of the channel depth of a MOSFET

In Fig. 12a, when $v_{GS} = V_t + V_{OV}$, applying v_{DS} causes the voltage drop along the channel to vary linearly, with an average value of $1/2 v_{DS}$ at the midpoint. Since $v_{GD} > V_t$, the channel still exists at the drain end. Fig. 12b shows the channel shape corresponding to the situation in Fig. 12a. While the depth of the channel at the source end is still proportional to V_{OV} , that at the drain end is proportional to $(V_{OV} - v_{DS})$.

Non-linearity explanation

- **step4** Define i_{DS} in terms of v_{DS} and v_{OV}.
  - Without tapering of the charge, if v_{OV} is independent of x, the area under the curve is $vOVL$. But with tapering, by using the area of a trapezoid, this area evaluates to $(V_{OV} - 1/2 v_{DS})L$
  - Previously, we saw that i_D is defined by Equation (19)

$$\begin{aligned} i_D &= \left[\mu_n C_{ox} \frac{W}{L} \left(v_{OV} - 1/2 v_{DS}\right)\right] v_{DS} \\ &= \left[\mu_n C_{ox} \frac{W}{L} \left(v_{OV} v_{DS} - 1/2 v_{DS}^2\right)\right] \end{aligned} \tag{19}$$

  - Since now $v_{OV} = v_{GS} - V_t$, then Equation (19) becomes

$$\begin{aligned} i_D &= \mu_n C_{ox} \frac{W}{L} \left[(v_{GS} - V_t) v_{DS} - 1/2 v_{DS}^2\right) \\ &= k_n' \frac{W}{L} \left[(v_{GS} - V_t) v_{DS} - 1/2 v_{DS}^2\right) \end{aligned} \tag{20}$$

  - Notice that when v_{DS} is small, the quadratic term can be dropped and we end up with the small v_{DS} equation.

Operation for $v_{DS} \geq v_{OV}$

Channel Pinch-Off and Current Saturation

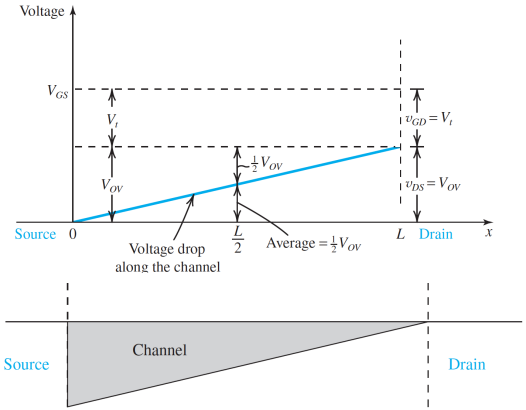


FIG 13. Operation of MOSFET with $v_{GS} = V_t + V_{OV}$
When $v_{DS} = V_{OV}$, at the drain end, v_{GD} decreases to V_t and the channel depth at the drain end reduces to zero (pinch-off). At this point, the MOSFET enters the saturation mode of operation. Further increasing v_{DS} has no effect on the channel shape and i_D remains constant.

Channel Pinch-Off and Current Saturation

- When $v_{DS} = V_{OV}$, then the channel depth is zero near the drain end
- At this junction, increasing v_{DS} does not increase the drain current i_D

$$i_{Dsat} = \frac{1}{2} k' \frac{W}{L} V_{OV}^2 \tag{21}$$

- The saturation voltage is given by

$$V_{DSsat} = V_{OV} = V_{GS} - V_t \tag{22}$$

- In general, as a function of v_{OV} , in the saturation region,

$$\begin{aligned} i_D &= \tfrac{1}{2} k_n' \tfrac{W}{L} v_{OV}^2 \\ &= \tfrac{1}{2} k_n' \tfrac{W}{L} (v_{GS} - V_t)^2 \end{aligned} \tag{23}$$

- In the saturation region, the relation between i_{DS} and v_{GS} is nonlinear.

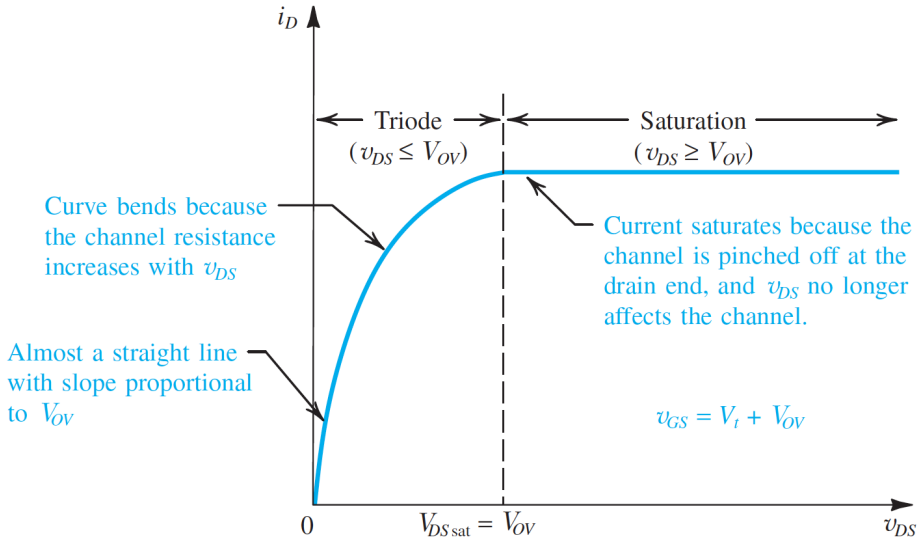


FIG 14. The drain current i_D versus the drain-to-source voltage v_{DS} for an NMOS transistor operated with $v_{GS} = V_t + V_{OV}$

The p and Complementary MOSFET

The p-Channel MOSFET

A PMOS can be made by replacing p region with n region and vice versa

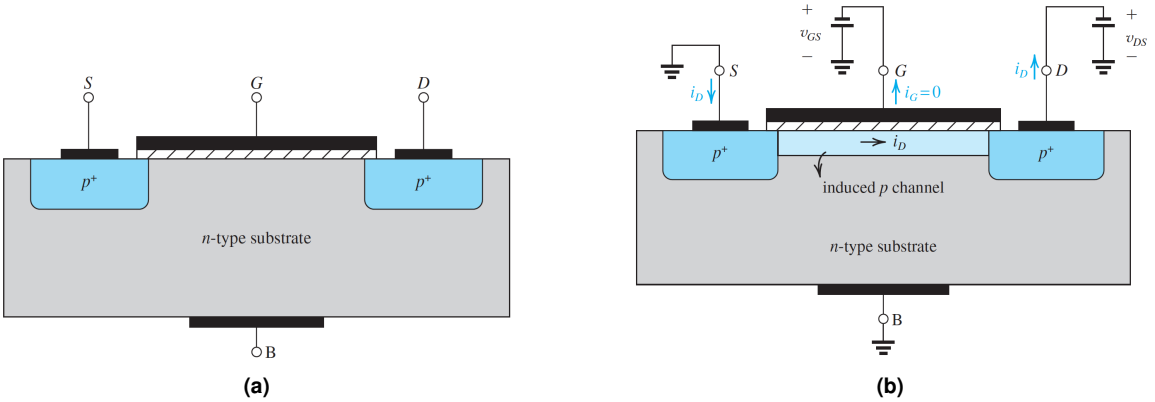


FIG 15. Physical structure of the PMOS transistor

Note that it is similar to the NMOS transistor except that all semiconductor regions are reversed in polarity. Fig. 15b shows the effect of a negative voltage v_{GS} of magnitude greater than V_{tp}. This negative voltage induces a p-channel, and a negative v_{DS} causes a current i_D to flow from source

The complementary MOS of CMOS

CMOS employs MOS transistors of both polarities.

- more difficult to fabricate
- more powerful and flexible
- now more prevalent than NMOS or PMOS

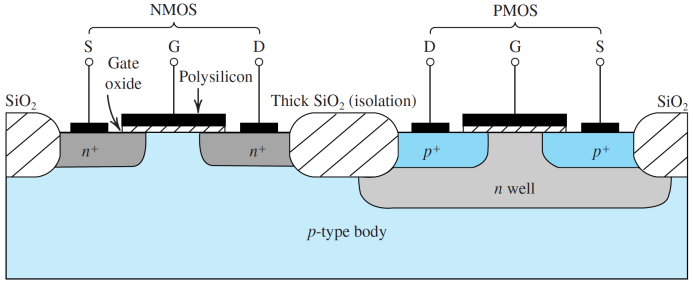


FIG 16. Cross section of a CMOS integrated circuit.
Note that the PMOS transistor is formed in a separate n-type region, known as an n well. Another arrangement is also possible in which an n-type substrate (body) is used and the n device is formed in a p well. Not shown are the connections made to the p-type body and to the n well; the latter functions as the body terminal for the p-channel device.

End