UNIVERSITY OF RWANDA
College of Science & Technology
School of Engeering
Department of Electrical & Electronics Engineering

Kizito NKURIKIYEYEZU, PhD

EPE 2165—Analog Electronics

SOLUTION #—2: DIODE CIRCUITS

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5.1

(a)

$$L = 1.5L_{\text{min}} = 1.5 \times 0.13 = 0.195\ \mu\text{m}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

where

$$\begin{aligned}\epsilon_{ox} &= 3.9\,\epsilon_0 = 3.9 \times 8.854 \times 10^{-12} \\ &= 3.45 \times 10^{-11}\ \text{F/m} \\ C_{ox} &= \frac{3.45 \times 10^{-11}\ \text{F/m}}{2.7 \times 10^{-9}\ \text{m}} \\ &= 1.28 \times 10^{-2}\ \text{F/m}^2 \\ &= 1.28 \times 10^{-2} \times 10^{15} \times 10^{-12}\ \text{fF}/\mu\text{m}^2 \\ &= 12.8\ \text{fF}/\mu\text{m}^2 \\ k_n' &= \mu_n C_{ox} \\ &= 400\ (\text{cm}^2/\text{V}\cdot\text{s}) \times 12.8\ (\text{fF}/\mu\text{m}^2) \\ &= 400 \times 10^8\ (\mu\text{m}^2/\text{V}\cdot\text{s}) \times 12.8 \times 10^{-15}\ (\text{F}/\mu\text{m}^2) \\ &= 512 \times 10^{-6}(\text{F/V}\cdot\text{s}) = 512 \times 10^{-6}\ (\text{A/V}^2) \\ &= 512\ \mu\text{A/V}^2 \\ k_n &= k_n'\ (W/L) \\ &= 512 \times \frac{1.3}{0.195} = 3413\ \mu\text{A/V}^2 \\ k_n &= 3.413\ \text{mA/V}^2\end{aligned}$$

(b) When the MOSFET operates in saturation, we have

$$I_D = \frac{1}{2}\,k_n V_{OV}^2$$

Thus,

$$100 = \frac{1}{2} \times 3413 \times V_{OV}^2$$

$$\Rightarrow V_{OV} = 0.24\ \text{V}$$

To operate in saturation, V_{DS} must at least be equal to V_{OV}, thus

$$V_{DS\text{min}} = 0.24\ \text{V}$$

The gate-to-source voltage is

$$V_{GS} = V_{tn} + V_{OV} = 0.4 + 0.24 = 0.64\ \text{V}$$

(c) When v_{DS} is small,

$$i_D \simeq k_n V_{OV}\, v_{DS}$$

and

$$r_{DS} \equiv \frac{v_{DS}}{i_D} = 1/k_n V_{OV}$$

Thus, for $r_{DS} = 2\ \text{k}\Omega$,

$$2 \times 10^3 = \frac{1}{3.413 \times 10^{-3}\ V_{OV}}$$

$$\Rightarrow V_{OV} = 0.15\ \text{V}$$

and, correspondingly,

$$V_{GS} = 0.4 + 0.15 = 0.55\ \text{V}$$

If V_{GS} is doubled, we obtain

$$V_{GS} = 2 \times 0.55 = 1.1\ \text{V}$$

and

$$V_{OV} = 1.1 - 0.4 = 0.7\ \text{V}$$

Thus, correspondingly, r_{DS} becomes

$$r_{DS} = \frac{1}{k_n V_{OV}} = \frac{1}{3.413 \times 10^{-3} \times 0.7}$$

$$= 418.6\ \Omega$$

As V_{GS} is reduced, r_{DS} increases, becoming infinite when the channel disappears, which occurs as V_{OV} reaches zero or, correspondingly,

$$V_{GS} = V_{tn} = 0.4 \text{ V}$$

5.2

(a) When the transistor operates in saturation, we obtain

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)V_{OV}^2$$

where

$$\begin{aligned}\mu_n C_{ox} &= 450\ (\text{cm}^2/\text{V·s}) \times 12.8\ (\text{fF}/\mu\text{m}^2)\\ &= 450 \times 10^8 (\mu\text{m}^2/\text{V·s}) \times 12.8 \times 10^{-15} (\text{F}/\mu\text{m}^2)\\ &= 576 \times 10^{-6} (\text{F/V·s})\\ &= 576\ \mu\text{A/V}^2\end{aligned}$$

To obtain $I_D = 100\ \mu$A, V_{OV} can be found from

$$100 = \frac{1}{2} \times 576 \times \frac{2\ \mu\text{m}}{0.2\ \mu\text{m}} \times V_{OV}^2$$

$$\Rightarrow V_{OV} = 0.186 \text{ V}$$

Correspondingly,

$$V_{GS} = V_{tn} + V_{OV} = 0.4 + 0.186 = 0.586 \text{ V}$$

At the edge of saturation,

$$V_{DS} = V_{DS\min} = V_{OV} = 0.186 \text{ V}$$

(b) If V_{DS} is lowered below $V_{DS\min}$, the transistor operates in the triode region, thus

$$\begin{aligned}i_D &= \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS} - V_{tn})\, v_{DS} - \frac{1}{2}v_{DS}^2\right]\\ &= 576 \times \frac{2}{0.2}\,(0.186 v_{DS} - 0.5 v_{DS}^2)\end{aligned}$$

For

$$v_{DS} = 0.5\ V_{DS\min} = 0.5 \times 0.186 = 0.093 \text{ V}$$

we obtain

$$\begin{aligned}i_D &= 576 \times 10\,(0.186 \times 0.093 - 0.5 \times 0.093^2)\\ &= 74.7\ \mu\text{A}\end{aligned}$$

For

$$v_{DS} = 0.1\ V_{DS\min} = 0.1 \times 0.186 = 0.0186 \text{ V}$$

we get

$$\begin{aligned}i_D &= 576 \times 10\,(0.186 \times 0.0186 - 0.5 \times 0.0186^2)\\ &= 18.9\ \mu\text{A}\end{aligned}$$

(c) For $V_{GS} = 0.6$ V (i.e., $V_{OV} = 0.2$ V) and $V_{DS} = 0.3$ V, the MOSFET will be operating in saturation with

$$\begin{aligned}I_D &= \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)V_{OV}^2\\ &= \frac{1}{2} \times 576 \times \frac{2}{0.2} \times 0.2^2\\ &= 115.2\ \mu\text{A}\end{aligned}$$

Now, if v_{GS} is increased by a 10-mV increment, then

$$v_{GS} = 0.6 + 0.010 = 0.610 \text{ V}$$

and the current becomes

$$i_D = \frac{1}{2} \times 576 \times \frac{2}{0.2} \times (0.610 - 0.4)^2$$

$$= 127\ \mu\text{A}$$

Thus, i_D increases by an increment

$$\triangle i_D = 127 - 115.2 = 11.8\ \mu\text{A}$$

If v_{GS} is decreased by 10 mV, we obtain

$$v_{GS} = 0.6 - 0.010 = 0.590 \text{ V}$$

and the current becomes

$$i_D = \frac{1}{2} \times 576 \times \frac{2}{0.2} \times (0.590 - 0.4)^2$$

$$= 104\ \mu\text{A}$$

Thus, the change in i_D is

$$\triangle i_D = 104 - 115.2 = -11.2\ \mu\text{A}$$

Observe that the incremental changes in i_D are almost equal, indicating that the operation is almost linear. Linearity improves if the incremental changes in v_{GS} are made smaller. (For instance, try $\triangle v_{GS} = \pm 5$ mV.)

5.3

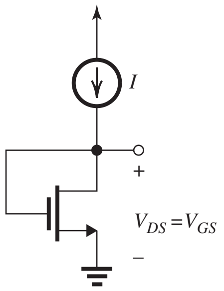

Figure 5.3.1

Refer to Fig. 5.3.1 and observe that since $V_{DS} = V_{GS} = V_t + V_{OV}$, we have

$$V_{DS} > V_{OV}$$

and thus the MOSFET is operating in the saturation region. Thus, ignoring channel-length modulation, we can write

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2$$

Substituting the given data, we obtain

$$40 = \frac{1}{2} \times 400 \times \left(\frac{W}{L}\right) (0.6 - V_t)^2 \qquad (1)$$

and

$$90 = \frac{1}{2} \times 400 \times \left(\frac{W}{L}\right) (0.7 - V_t)^2 \qquad (2)$$

Dividing Eq. (2) by Eq. (1), we obtain

$$\frac{9}{4} = \frac{(0.7 - V_t)^2}{(0.6 - V_t)^2}$$
$$\Rightarrow \frac{3}{2} = \frac{0.7 - V_t}{0.6 - V_t}$$

which results in

$$V_t = 0.4 \text{ V}$$

Substituting for V_t into Eq. (1) gives

$$40 = 200 \times \left(\frac{W}{L}\right) \times 0.04$$
$$\Rightarrow \frac{W}{L} = 5$$

5.4

Operation with $V_{DS} = V_{GS} = V_t + V_{OV}$ means $V_{DS} > V_{OV}$ and thus the MOSFET is in the saturation region. Thus, neglecting channel-length modulation, we can write for I_D,

$$I_D = \frac{1}{2} k_n (V_{GS} - V_t)^2$$
$$= \frac{1}{2} \times 4 \times (0.6 - 0.35)^2$$
$$= 0.125 \text{ mA}$$

The voltage V_{DS} can be reduced to a value equal to V_{OV} while the MOSFET remains in the saturation region, that is,

$$V_{DS\min} = 0.6 - 0.35 = 0.25 \text{ V}$$

A transistor having twice the value of W will have twice the value of k_n and thus the current will be twice as large, that is,

$$I_D = 2 \times 0.125 = 0.25 \text{ mA}$$

The linear resistance r_{DS} is given by

$$r_{DS} = \frac{1}{k_n (V_{GS} - V_t)}$$

With $V_t = 0.35$ V and with V_{GS} varying over the range 0.5 V to 1 V, r_{DS} will vary over the range

$$r_{DS} = \frac{1}{0.15\, k_n} \text{ to } \frac{1}{0.65\, k_n}$$

For the first device with $k_n = 4$ mA/V, r_{DS} will vary over the range

$$r_{DS} = \frac{1}{0.15 \times 4} = 1.67 \text{ k}\Omega$$

to

$$r_{DS} = \frac{1}{0.65 \times 4} = 0.38 \text{ k}\Omega$$

The wider device has $k_n = 8$ mA/V and thus its r_{DS} will vary over the range

$$r_{DS} = 0.833 \text{ k}\Omega \text{ to } 0.192 \text{ k}\Omega$$

5.5

(a)

$$V_A = V_A' L = 5 \times 0.26 = 1.3 \text{ V}$$
$$\lambda = \frac{1}{V_A} = \frac{1}{1.3} = 0.77 \text{ V}^{-1}$$

(b) Since $V_{DS} = 0.65$ V is greater than V_{OV}, the NMOS transistor is operating in saturation. Thus,

$$I_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)V_{OV}^2(1+\lambda V_{DS})$$
$$= \frac{1}{2} \times 500 \times \frac{2.6}{0.26} \times 0.2^2 \times (1+0.77\times 0.65)$$
$$= 150 \text{ µA}$$

(c)

$$r_o = \frac{V_A}{I_D'}$$

where I_D' is the drain current without taking channel-length modulation into account, thus

$$I_D' = \frac{1}{2}k_n'\left(\frac{W}{L}\right)V_{OV}^2$$
$$= \frac{1}{2} \times 500 \times \frac{2.6}{0.26} \times 0.2^2$$
$$= 100 \text{ µA}$$

Hence,

$$r_o = \frac{1.3 \text{ V}}{100 \text{ µA}} = \frac{1.3 \text{ V}}{0.1 \text{ mA}} = 13 \text{ k}\Omega$$

(d) If V_{DS} is increased to 1.3 V, I_D becomes

$$I_D = \frac{1}{2} \times 500 \times \frac{2.6}{0.26} \times 0.2^2 \,(1+0.77\times 1.3)$$
$$= 200 \text{ µA}$$

That is, I_D increases by 50 µA. Alternatively, we can use r_o to determine the increase in I_D as

$$\triangle I_D = \frac{\triangle V_{DS}}{r_o}$$
$$= \frac{0.65 \text{ V}}{13 \text{ k}\Omega} = 0.05 \text{ mA} = 50 \text{ µA}$$

which is identical to the result obtained directly.

5.6

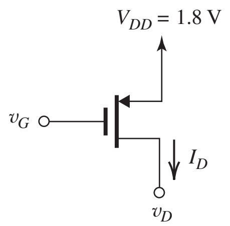

Figure 5.6.1

$$V_{tp} = -0.5 \text{ V}, \qquad k_p' = 100 \text{ µA/V}^2$$
$$W/L = 10$$

(a) For the transistor to conduct, v_G must be lower than v_S by at least $|V_{tp}|$, that is, by 0.5 V. Thus, the transistor conducts for $v_G \le 1.8 - 0.5$, or $v_G \le$ 1.3 V.

(b) For the transistor to operate in the triode region, the drain voltage must be higher than the gate voltage by at least $|V_{tp}|$ volts, thus

$$v_D \ge v_G + 0.5 \text{ V}$$

(c) For the transistor to operate in the saturation region, the drain voltage cannot exceed the gate voltage by more than $|V_{tp}|$, that is,

$$v_D \le v_G + 0.5 \text{ V}$$

(d) When the transistor is operating in saturation, we obtain

$$I_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)|V_{OV}|^2$$

Substituting the given values, we obtain

$$20 = \frac{1}{2} \times 100 \times 10|V_{OV}|^2$$
$$\Rightarrow |V_{OV}| = 0.2 \text{ V}$$

which is obtained when

$$v_G = V_{DD} - V_{SG}$$
$$= 1.8 - (|V_{tp}| + |V_{OV}|)$$
$$= 1.8 - (0.5 + 0.2) = 1.1 \text{ V}$$

For this value of v_G, the range that v_D is allowed to have while the transistor remains in saturation is

$$v_D \le v_G + |V_{tp}|$$

that is,

$$v_D \le 1.6\text{ V}$$

(e)

$$r_o = \frac{|V_A|}{I'_D} = \frac{1}{|\lambda| I'_D}$$

where I'_D is the value of I_D without channel-length modulation taken into account, that is,

$$I'_D = \frac{1}{2}k'_p\left(\frac{W}{L}\right)|V_{OV}|^2$$
$$= \frac{1}{2} \times 100 \times 10 \times 0.2^2 = 20\ \mu\text{A}$$

Thus,

$$r_o = \frac{1}{0.2 \times 20} = 0.25\ \text{M}\Omega$$

(f)

$$I_D = \frac{1}{2}k'_p\left(\frac{W}{L}\right)V_{OV}^2(1 + |\lambda|V_{SD})$$

At $V_D = 1$ V, we have $V_{SD} = 1.8 - 1 = 0.8$ V, and

$I_D = \frac{1}{2} \times 100 \times 10 \times 0.2^2(1 + 0.2 \times 0.8) =$ 23.2 μA.

At $V_D = 0$ V, we get $V_{SD} = 1.8 - 0 = 1.8$ V, and

$I_D = \frac{1}{2} \times 100 \times 10 \times 0.2^2\ (1 + 0.2 \times 1.8) = 27.2\ \mu\text{A}$

Thus, for

$$\triangle V_{SD} = 1.8 - 0.8 = 1\text{ V},$$

the current changes by

$$\triangle I_D = 27.2 - 23.2 = 4\ \mu\text{A}$$

indicating that the output resistance r_o is

$$r_o = \frac{\triangle V_D}{\triangle I_D} = \frac{1\text{ V}}{4\ \mu\text{A}} = 0.25\ \text{M}\Omega$$

which is the same value found in (e).

5.7

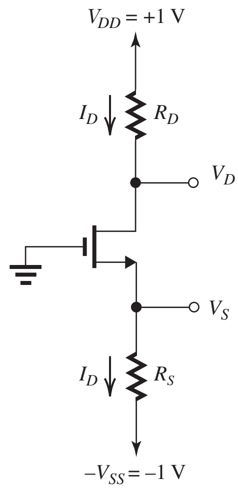

Figure 5.7.1

(a) Refer to the circuit in Fig. 5.7.1. For $V_D = +0.5$ V, the transistor is operating in saturation since $V_D > V_G$. Thus,

$$I_D = \frac{1}{2}k'_n\left(\frac{W}{L}\right)V_{OV}^2$$

where we have utilized the given information that $\lambda = 0$. To obtain $I_D = 180\ \mu$A, the required V_{OV} can be found from

$$180 = \frac{1}{2} \times 400 \times 10V_{OV}^2$$
$$\Rightarrow V_{OV} = 0.3\text{ V}$$

The value of V_{GS} can be found as

$$V_{GS} = V_{tn} + V_{OV} = 0.5 + 0.3 = 0.8\text{ V}$$

from which V_S can be determined as

$$V_S = V_G - V_{GS} = 0 - 0.8 = -0.8\text{ V}$$

The required value of R_S can now be found from

$$R_S = \frac{V_S - (-V_{SS})}{I_D}$$
$$= \frac{-0.8 - (-1)}{180\ \mu\text{A}} = \frac{0.2\text{ V}}{0.18\text{ mA}} = 1.11\text{ k}\Omega$$

Finally, the value of R_D can be found from

$$R_D = \frac{V_{DD} - V_D}{I_D}$$
$$= \frac{1 - 0.5}{0.18\text{ mA}} = 2.78\text{ k}\Omega$$

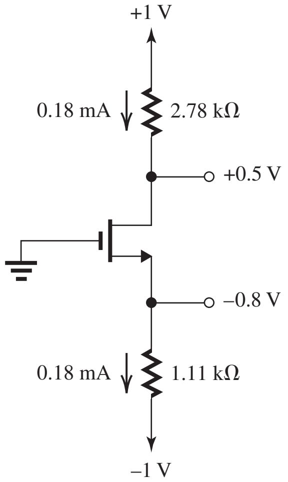

Figure 5.7.3

Figure 5.7.3 shows the designed circuit with the component values and the values of current and voltages.
(b) If R_S is replaced by a constant-current source I, as shown in Fig. 5.7.2, the value of I must be equal to the desired value of I_D, that is, 180 µA or 0.18 mA.

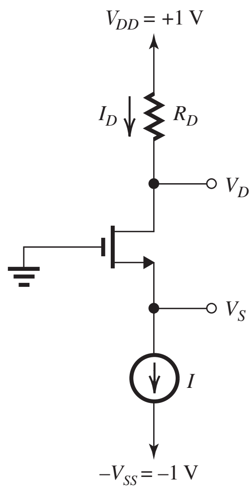

Figure 5.7.2

(c) Refer to Fig. 5.7.1. As R_D is is increased, V_D decreases as

$$V_D = 1 - I_D R_D$$
$$= 1 - 0.18 R_D$$

Eventually, V_D falls below V_G by V_{tn} at which point the transistor leaves the saturation region and enters the triode region. This occurs at

$$V_D = V_G - V_{tn} = 0 - 0.5 = -0.5\text{ V}$$

The corresponding value of R_D can be found from

$$-0.5 = 1 - 0.18 \times R_D$$
$$\Rightarrow R_D = 8.33\text{ k}\Omega$$

5.8

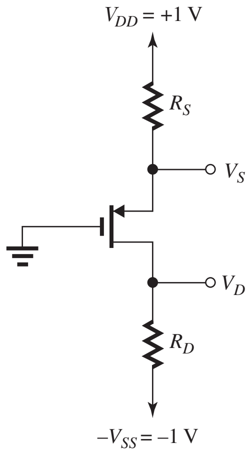

Figure 5.8.1

(a) With $V_D = 0$ V, the transistor will be operating in the saturation region since $V_D = V_G$. Thus,

$$I_D = \frac{1}{2} k_p' \left(\frac{W}{L}\right) |V_{OV}|^2$$

where we have taken into account that $\lambda = 0$ as stated. To obtain $I_D = 0.1$ mA $= 100$ µA, the required value of $|V_{OV}|$ can be found as follows:

$$100 = \frac{1}{2} \times 100 \times 20 |V_{OV}|^2$$
$$\Rightarrow |V_{OV}| = 0.316\text{ V}$$

The value of V_{SG} can now be found as

$$V_{SG} = |V_{tp}| + |V_{OV}| = 0.5 + 0.316 = 0.816 \text{ V}$$

Thus,

$$V_S = V_{SG} = 0.816 \text{ V}$$

The required value of R_S can be determined from

$$R_S = \frac{V_{DD} - V_S}{I_D} = \frac{1 - 0.816}{0.1} = 1.84 \text{ k}\Omega$$

Finally, the required value of R_D can be found from

$$R_D = \frac{V_D - (-V_{SS})}{I_D} = \frac{0 - (-1)}{0.1} = 10 \text{ k}\Omega$$

The designed circuit with component values and current and voltage values is shown in Figure 5.8.2. The reader can check the calculations directly on the circuit diagram.

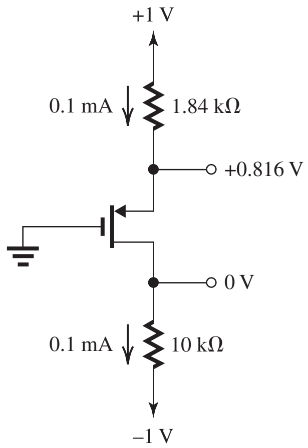

Figure 5.8.2

(b) Refer to Figure 5.8.1. The transistor remains in saturation as long as V_D does not increase above V_G by more than $|V_{tp}|$. Since $V_G = 0$ and $|V_{tp}| = 0.5$ V, the maximum allowable value of V_D is

$$V_{D\max} = +0.5 \text{ V}$$

To obtain this value of V_D, R_D must be increased to

$$R_D = \frac{V_{D\max} - (-1)}{0.1 \text{ mA}} = \frac{0.5 + 1}{0.1} = 15 \text{ k}\Omega$$

5.9

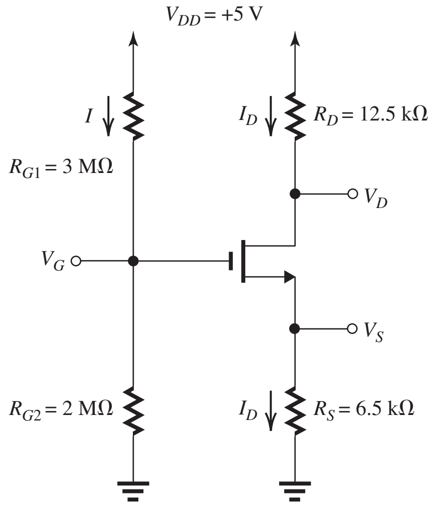

Figure 5.9.1

The current I through the voltage divider R_{G1}–R_{G2} can be found as

$$I = \frac{V_{DD}}{R_{G1} + R_{G2}} = \frac{5 \text{ V}}{3 \text{ M}\Omega + 2 \text{ M}\Omega} = \frac{5 \text{ V}}{5 \text{ M}\Omega} = 1 \ \mu\text{A}$$

The voltage V_G at the gate can now be found as

$$V_G = IR_{G2} = 1 \ \mu\text{A} \times 2 \text{ M}\Omega = 2 \text{ V}$$

The voltage V_S is given by

$$V_S = V_G - V_{GS} = V_G - (V_t + V_{OV}) = 2 - (0.5 + V_{OV})$$

$$V_S = 1.5 - V_{OV} \qquad (1)$$

But V_S can be expressed in terms of I_D as

$$V_S = I_D R_S = I_D \times 6.5 = 6.5 I_D$$

Thus,

$$6.5 I_D = 1.5 - V_{OV} \qquad (2)$$

We do not know whether the transistor is operating in the saturation region or in the triode region. Therefore, we must make an assumption about the region of operation, complete the analysis, and then use the results obtained to check the validity of our assumption. If our assumption proves valid, our work is done. Otherwise, we must redo the analysis assuming the other mode of operation. Since the *i*–*v* relationships that describe the saturation-region operation are simpler than those that apply in the triode region, we normally assume operation in the saturation region, unless of course there is an indication of triode-mode operation.

Assuming that the transistor in the circuit of Figure 5.9.1 is operating in saturation, we can write

$$I_D = \frac{1}{2}k_n V_{OV}^2 = \frac{1}{2} \times 10V_{OV}^2$$

$$I_D = 5V_{OV}^2 \qquad (3)$$

Substituting for I_D from Eq. (3) into Eq. (2) gives

$$6.5 \times 5V_{OV}^2 = 1.5 - V_{OV}$$

which can be rearranged into the form

$$32.5V_{OV}^2 + V_{OV} - 1.5 = 0$$

Solving this quadratic equation yields

$$V_{OV} = 0.2 \text{ V or } -0.23 \text{ V}$$

Obviously, the negative value is physically meaningless and can be discarded. Thus,

$$V_{OV} = 0.2 \text{ V}$$

and

$$I_D = 5V_{OV}^2 = 5 \times 0.2^2 = 0.2 \text{ mA}$$

We are now ready to check the validity of our assumption of saturation mode operation. Referring to the circuit in Figure 5.9.1, we can find the voltage V_D as follows:

$$V_D = V_{DD} - I_D R_D$$
$$= 5 - 0.2 \times 12.5 = 2.5 \text{ V}$$

which is greater than V_G (2 V), confirming that the transistor is operating in saturation, as assumed. Figure 5.9.2 shows the circuit together with the values of all node voltages and branch currents. The reader is encouraged to check their results by doing a few calculations directly on the circuit.

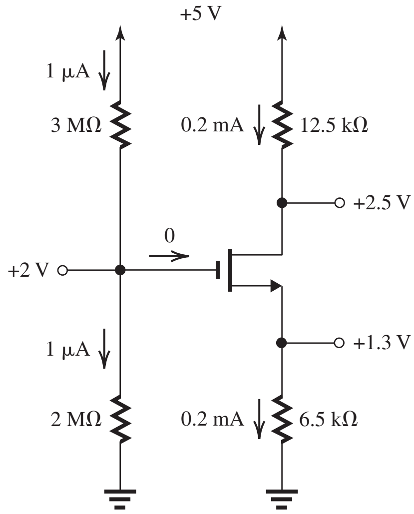

Figure 5.9.2

5.10

From Fig. 5.10.1 in the problem statement we observe that transistor Q_1 together with its associated resistors is an identical circuit to that analyzed in the solution to Problem 5.9 (see Fig. 5.9.1). Since the gate terminal of Q_2 draws zero current, transistor Q_2 together with its associated resistances do **not** change the currents and voltages in Q_1 and its associated resistances. Thus, we need to only concern ourselves with the analysis of the part of the circuit shown in Figure 5.10.2, where V_{GS} is found from

$$V_{G2} = V_{D1} = 2.5 \text{ V}$$

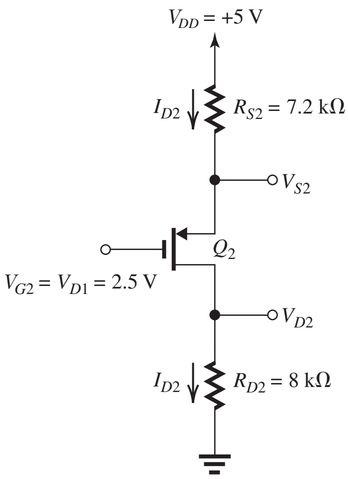

Figure 5.10.2