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EPE 2165—Analog Electronics

EXERCISE #—2: MOSFET CIRCUITS

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Section 5.1: Device Structure and Physical Operation

5.1

An NMOS transistor is fabricated in a 0.13-μm CMOS process with $L = 1.5L_{\text{min}}$ and $W = 1.3$ μm. The process technology is specified to have $t_{ox} = 2.7$ nm, $\mu_n = 400\,\text{cm}^2/\text{V·s}$, and $V_{tn} = 0.4$ V.

(a) Find C_{ox}, k'_n, and k_n.

(b) Find the overdrive voltage V_{OV} and the minimum value of V_{DS} required to operate the transistor in saturation at a current $I_D = 100$ μA. What gate-to-source voltage is required?

(c) If v_{DS} is very small, what values of V_{OV} and V_{GS} are required to operate the MOSFET as a 2-kΩ resistance? If V_{GS} is doubled, what r_{DS} results? If V_{GS} is reduced, at what value does r_{DS} become infinite?

Section 5.2: Current–Voltage Characteristics

5.2

An NMOS transistor fabricated in a 0.13-μm process has $L = 0.2$ μm and $W = 2$ μm. The process technology has $C_{ox} = 12.8\,\text{fF}/\mu\text{m}^2$, $\mu_n = 450\,\text{cm}^2/\text{V·s}$, and $V_{tn} = 0.4$ V. Neglect the channel-length modulation effect.

(a) If the transistor is to operate at the edge of the saturation region with $I_D = 100$ μA, find the values required of V_{GS} and V_{DS}.

(b) If V_{GS} is kept constant at the value found in (a) while V_{DS} is changed, find I_D that results at V_{DS} equal to half the value in (a) and at V_{DS} equal to 0.1 the value in (a).

(c) To investigate the operation of the MOSFET as a linear amplifier, let the operating point be at $V_{GS} = 0.6$ V and $V_{DS} = 0.3$ V. Find the change in i_D for v_{GS} changing from 0.6 V by +10 mV and by −10 mV. Comment.

5.3

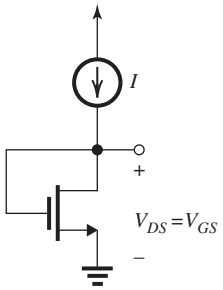

Figure 5.3.1

An NMOS transistor fabricated in a process for which the process transconductance parameter is $400\,\mu\text{A}/\text{V}^2$ has its gate and drain connected together. The resulting two-terminal device is fed with a current source I as shown in Fig. 5.3.1. With $I = 40$ μA, the voltage across the device is measured to be 0.6 V. When I is increased to 90 μA, the voltage increases to 0.7 V. Find V_t and W/L of the transistor. Ignore channel-length modulation.

5.4

An NMOS transistor for which $k_n = 4\,\text{mA}/\text{V}^2$ and $V_t = 0.35$ V is operated with $V_{GS} = V_{DS} = 0.6$ V. What current results? To what value can V_{DS} be reduced while maintaining the current unchanged? If the transistor is replaced with another fabricated in the same technology but

with twice the width, what current results? For each of the two transistors when operated at small V_{DS}, what is the range of linear resistance r_{DS} obtained when V_{GS} is varied over the range 0.5 V to 1 V? Neglect channel-length modulation.

5.5

An NMOS transistor is fabricated in a 0.13-μm process having $k'_n = 500\,\mu A/V^2$, and $V'_A = 5\,V/\mu m$.
(a) If $L = 0.26\,\mu m$ and $W = 2.6\,\mu m$, find V_A and λ.
(b) If the device is operated at $V_{OV} = 0.2\,V$ and $V_{DS} = 0.65\,V$, find I_D.
(c) Find r_o at the operating point specified in (b).
(d) If V_{DS} is increased to 1.3 V, what is the corresponding change in I_D? Do this two ways: using the expression for I_D and using r_o. Compare the results obtained.

5.6

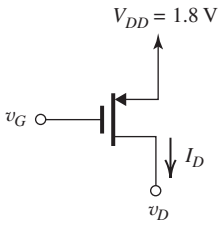

Figure 5.6.1

The PMOS transistor in Fig. 5.6.1 has $V'_{tp} = -0.5\,V$, $k'_p = 100\,\mu A/V^2$, and $W/L = 10$.
(a) Find the range of v_G for which the transistor conducts.
(b) In terms of v_G, find the range of v_D for which the transistor operates in the triode region.
(c) In terms of v_G, find the range of v_D for which the transistor operates in saturation.
(d) Find the value of v_G and the range of v_D for which the transistor operates in saturation with $I_D = 20\,\mu A$. Assume $\lambda = 0$.
(e) If $|\lambda| = 0.2\,V^{-1}$, find r_o at the operating point in (d).
(f) For V_{OV} equal to that in (d) and $|\lambda| = 0.2\,V^{-1}$, find the value of I_D at $V_D = 1\,V$ and at $V_D = 0\,V$. Use these values to calculate the output resistance r_o and compare the result to that found in (e).

Section 5.3: MOSFET Circuits at DC

D5.7

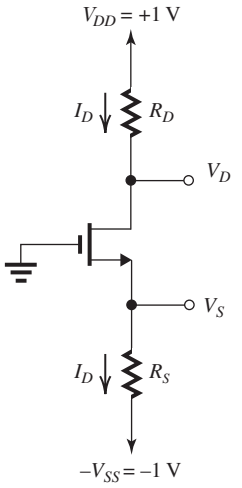

Figure 5.7.1

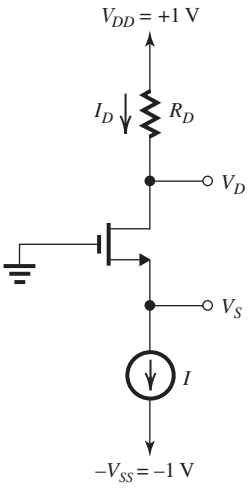

Figure 5.7.2

The NMOS transistor in the circuit in Fig. 5.7.1 has $V_{tn} = 0.5\,V$, $k'_n = 400\,\mu A/V^2$, $W/L = 10$, and $\lambda = 0$.
(a) Design the circuit (i.e., find the required values for R_S and R_D) to obtain $I_D = 180\,\mu A$ and $V_D = +0.5\,V$. Find the voltage V_S that results.
(b) If R_S is replaced with a constant-current source I, as shown in Fig. 5.7.2, what must the value of I be to obtain the same operating conditions as in (a)?
(c) What is the largest value to which R_D can be increased while the transistor remains in saturation?

D5.8

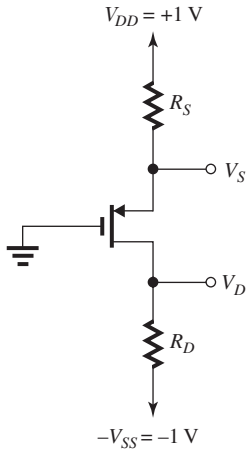

Figure 5.8.1

The PMOS transistor in the circuit in Fig. 5.8.1 has $V_{tp} = -0.5$ V, $k'_p = 100$ μA/V^2, $W/L = 20$, and $\lambda = 0$.
(a) Find R_S and R_D to obtain $I_D = 0.1$ mA and $V_D = 0$ V.
(b) What is the largest R_D for which the transistors remains in saturation. At this value of R_D, what is the voltage at the drain, V_D?

5.9

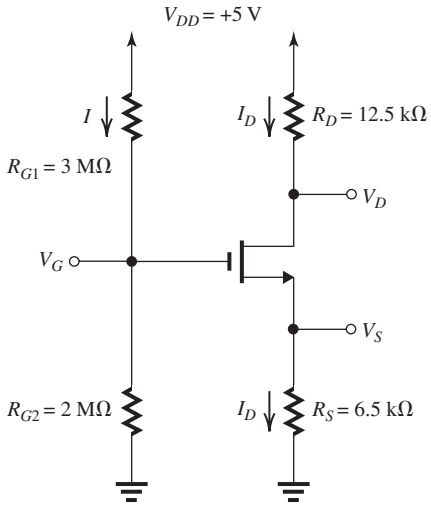

Figure 5.9.1

The NMOS transistor in the circuit in Fig. 5.9.1 has $V_t = 0.5$ V, $k_n = 10$ mA/V^2, and $\lambda = 0$. Analyze the circuit to determine the currents through all branches and to find the voltages at all nodes.

5.10

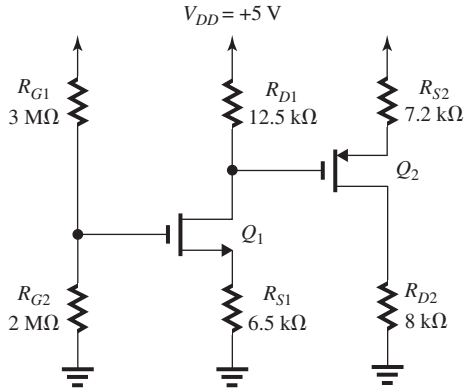

Figure 5.10.1

For the circuit in Fig. 5.10.1, the NMOS transistor has $V_{tn} = 0.5$ V, $k_n = 10$ mA/V^2, and $\lambda_n = 0$, and the PMOS transistor has $V_{tp} = -0.5$ V, $k_p = 12.5$ mA/V^2, and $|\lambda_p| = 0$. Observe that Q_1 and its surrounding circuit is the same as the circuit analyzed in Problem 5.9 (Fig. 5.9.1), and you may use the results found in the solution to that problem here. Analyze the circuit to determine the currents in all branches and the voltages at all nodes.

D5.11

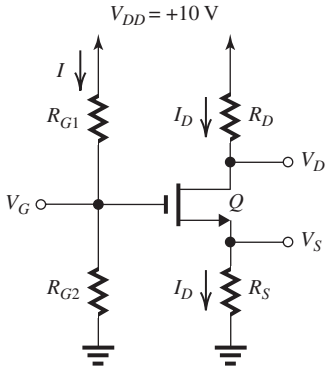

Figure 5.11.1

Design the circuit in Fig. 5.11.1 to obtain $I = 1$ μA, $I_D = 0.5$ mA, $V_S = 2$ V, and $V_D = 5$ V. The NMOS transistor has $V_t = 0.5$ V, $k_n = 4$ mA/V^2, and $\lambda = 0$.

5.12

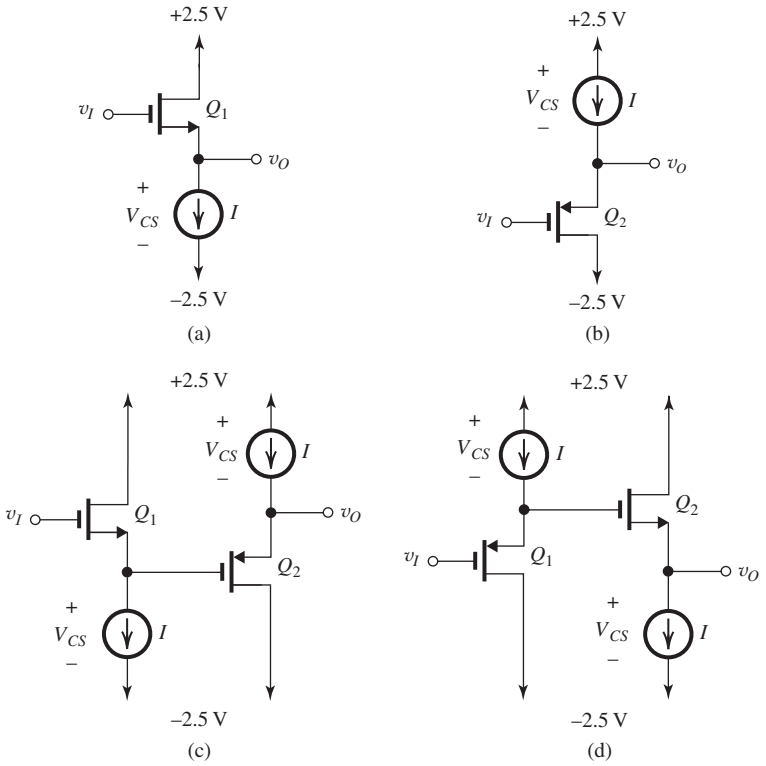

Figure 5.12.1

The transistors in the circuits of Fig. 5.12.1 have $|V_t| = 0.5$ V, $k_n = k_p = 20\,\text{mA/V}^2$, and $\lambda = 0$. Also, $I = 0.9$ mA. For each circuit find v_O as a function of v_I assuming the transistors are operating in saturation. In each case find the allowable ranges of v_O and v_I. Assume that the minimum voltage V_{CS} required across each current source is 0.3 V.